PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Algirdas Avizienis	Before the Board of Patent Appeals and Interferences
Serial No.:	09/886,959	
Filed:	June 20, 2001	
Title:	"SELF-TESTING AND -REPAIRING FAULT-TOLERANCE INFRASTRUC-TURE FOR COMPUTER SYSTEMS"	
Our docket:	xAAA-02	Examiner Bryce P. Bonzo Art Unit 2113

APPEAL BRIEF

Hon. Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is pursuant to the Applicant/Appellant's Notice of Appeal filed on November 24, 2006.

Attached are a check to cover the Appeal-Brief fee in the amount of $250; and an acknowledgment card for date-stamping and return.

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(1) IDENTIFICATION PAGE;

Identification data for this case appear above. Following this "Identification Page", Appellant provides a "Table of Contents Page" which lists all other sections of this Brief.

CERTIFICATION OF EXPRESS MAIL DEPOSIT
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Signed:
Peter J. Lippman

(2) TABLE OF CONTENTS Page

As suggested in 69 Federal Register 155, bridging pages 49978 and 49979, each of the "items" in this Brief begins on a separate page, namely:

*These pages are also numbered as original pages 1 through 17 of the Declaration and of the listing, respectively.

(3) REAL PARTY IN INTEREST Page

The sole real party in interest is the inventor and Appellant, Dr. Algirdas Avizienis.

(4) RELATED APPEALS AND INTERFERENCES Page

There is no related appeal or interference.

(5) STATUS OF CLAIMS Page

Claim 84 was allowed in the Official Action of August 24, 2006.

Twelve claims have been canceled — namely, claims 25 through 32, and claims 39, 40, 60 and 72.

All the other claims stand rejected — namely, claims:

1 through 24,
33 through 38,
41 through 59,
61 through 71, and
73 through 83.

As further discussed on page 13, the Appellant respectfully asks to exclude from this appeal six claims: claims 62 through 64, and claims 76 through 78.

Thus the claims submitted on appeal are:

1 through 24,
33 through 38,
41 through 59,
61,
65 through 71,
73 through 75, and
79 through 83.

(6) STATUS OF AMENDMENTS Page

The five Amendments (and one Request for Reconsideration) listed below have been filed in this case, subsequent to the earliest Final Rejection (which is dated July 12, 2005). All the indicated dates are the dates of mailing:

- October 12, 2005 Amendment under Rule 116 (with Request for Continuing Examination);
- October 27, 2005 Supplemental Amendment under Rule 116 — ACKNOWLEDGED BY THE EXAMINER IN THE OFFICIAL ACTION OF JANUARY 13, 2006;
- May 15, 2006 Amendment;
- June 5, 2006 Further Response (filing the Declaration of Jean-Claude Laprie) — ACKNOWLEDGED BY THE EXAMINER IN THE OFFICIAL ACTION OF AUGUST 24, 2006;
- October 24, 2006 Request for Reconsideration (reasoning without amendment) — ACKNOWLEDGED BY EXAMINER BONZO IN THE ADVISORY ACTION OF NOVEMBER 13, 2006; and
- November 22, 2006 Further Supplemental Amendment (to the Specification only, with discussion of telephone interview with SPE Beausoliel).

All these papers appear in the PAIR website without Examiner objection and accordingly are believed to have been entered.

(7) SUMMARY OF CLAIMED SUBJECT MATTER Pages

INTRODUCTION — The invention defined by the Applicant's claims establishes a very general kind of novel configuration, or architecture, that is compatible with almost any computing system — to protect that system against failure. The protected computing system can be essentially conventional (as specified in some of the claims) — but may instead be specialized (as specified in others).

The objective of this invention, as claimed, is to enable essentially ordinary computing systems to function (without failing) for extremely long periods of time — such as hundreds and even thousands of years. Experts in the computer-science field, and particularly in its specialty subfields of reliability and fault-tolerance, have greeted this radical invention with admiration and in fact excitement.

Figuratively speaking, the novel architecture envelops the computing system in a protective sheath — that has numerous distinctly different characteristics, and that provides a variety of mechanisms for both checking and correcting operation of the system. These numerous characteristics and mechanisms are believed to be patentable independently, as well as, of course, in combination — and accordingly are recited both independently and in several crosscombinations, in the claims.

a) ALL THE CLAIMS IN COMMON — All of the claims recite, in substance: apparatus for deterring failure of a computing system; said apparatus comprising a network of components having terminals for connection to such system.

Essentially those words are used in all the independent claims except claim 81 — and allowed claim 84. In these latter claims, the "apparatus" is instead called an "infrastruc-

ture" and the "terminals" are instead called "at least one adapter node ('A-node')".

In the drawings, the "computing system" modules, being protected against failure, are marked "C" (Figs. 1 and 2) and sometimes also "11". The modules of the "network" or "apparatus" (which are doing the protecting, or "deterring" of failure) make up essentially all the rest of the drawings and are marked "M", "A", "S", "S3", "X" — and also variously "11" through "14" (Fig. 1), ""201a", "201b", "201c","202" and "203" (Fig. 2), as well as "601a", "601b" and "601c", "602" and "603" (Fig. 3) — except for the "terminals" which are "14" and "17".

b) DISTINCTION BETWEEN INVENTION AND ITS CONTEXT — In the independent claims, the protected computing system C, 11 is not an element of the claimed invention (of the independent claims). Nevertheless the claims necessarily refer to that protected system, particularly when defining elements of the invention by their relationships to that protected system.

Certain dependent claims, on the other hand, expressly define an enlarged claimed "combination" invention, of which that system is an element. Because this section of the Brief is required to provide a "Summary of Claimed Subject Matter", an explanatory comment is included here.

To make it absolutely clear that the protected "system" is not an element of the invention defined by the independent claims, but rather only an element of the operating environment of the invention, (1) the computing system is recited in the claim preambles; and (2) a special nomenclature has been used in the bodies of the claims, when referring back to the computing system. That nomenclature was explained in early Amendments, and is specifically defined in the November 22, 2006 Amendment to the Specification.

As stated in the Amendments — and in that newly added passage — the purpose of this usage is to make clear which

components of the overall assemblage are only parts of the environment, or context, of the invention, and which components are parts of the invention itself. Thus, this nomenclature furthers the mandate of 35 USC § 112 to provide claims "particularly pointing out and distinctly claiming" the invention.

Most patent practitioners may prefer to leave this distinction ambiguous, hoping to later resolve the ambiguity in favor of the patentee during litigation, or in licensing negotiations, after it has been learned what a putative infringer or prospective licensee is doing or wants to do. Under the present claiming philosophy, it is instead best to know that a competitor definitely can be an "infringer" (of the independent claims) even if s/he does not supply or use certain components — namely, here, the protected computing system.

The contrary is true under particular dependent claims. Often this is helpful for measure-of-damages purposes, if the infringer is also supplying the protected computing system.

This way, it is not necessary to deliberately leave anything ambiguous in the claims. The claims cover both possibilities expressly: the protected system is not an element of the claimed invention of the independent claims, but is part of the claimed invention of certain dependent claims.*

This nomenclature appears in a number of previously issued patents written and prosecuted by the undersigned. It has been accepted by the Board of Appeals in a case previously appealed by the undersigned, U. S. 6,176,616 of Joffe (claims 1, 6 and 17).

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*With apologies — during preparation of this paper six errors have been noted in use of this nomenclature: in claim 13, last paragraph only, "such" should be deleted [two occurrences]; and in claim 65, in the lines 8, 9, 13 and 14 only, "the" should read "such" (four occurrences). Applicant would hope to correct these points by amendment if these claims are allowed.

c) SPECIFIC INDEPENDENT CLAIMS — The several characteristics and mechanisms of the novel architecture occur in various combinations and crosscombinations, in the claims. Only a few claims recite just one of the characteristics.

- Claim 1: "hardware network" — The protective network has been introduced in section "a)" above. The facts that it is preferably all hardware, "having substantially no software and substantially no firmware" (with stated exceptions), and that it includes circuits that are "fabrication-preprogrammed" to guard the system against failure, are discussed in the Specification at, *e. g.*, page 7, line 17, through page 9 line 10; page 28, lines 2 through 5, and page 49 line 1. Reasons for this construction appear at, *e. g.*, page 31, lines 1 and 2; and at page 9, line 17, through page 10 line 5. Detailed <u>hardware</u> designs are shown in the Appellant's drawings: Figs. 3, 4a, 4b, 5, 7 and 9 — further evidence that the network is intended to be all hardware.

- Independent claims 13, 42 and 50: the network guards the "entire" system against failure — This feature is both implied by the drawings, which show a separate structural representation C, 11 for the entire protected system, and discussed in the Specification at, *e. g.*, page 31, lines 11 through 14, and page 35 line 1; with additional discussion at page 28, lines 14 through 16, page 29, lines 1 and 2, and page 33, lines 16 and 17.

- Claims 50, 55 and 81: the network is <u>distinct from</u> the computing system — This characteristic was inserted into the claims to distinguish a previously cited reference in which a system in essence protected only <u>itself</u>: there was no infrastructure or separate protective layer. This

feature too is implied by the separate structure C, 11 shown in the drawings for the protected system, and discussed in the Specification at, *e. g.*, the same points noted above for claims 13 ff.

- Claims 13, 42 and 50: protected system has parallel channels, or mutually redundant modules — The Specification at, *e. g.*, page 30, lines 6 through 14, and page 55, lines 14 through 17 (also *e. g.*, page 52 lines 16 through 18, as well as page 32 lines 10 and 11) makes clear that the several protected systems C, 11 are advantageously parallel or mutually redundant. (Also *cf.* claim 55 below, "plural processors".)

- Claim 13: network identifies and corrects failure of any of <u>its own</u> circuits — Unlike the above-mentioned previously cited art (in which a "protective" system protected itself <u>only</u>) this self-protective characteristic of the protective network is <u>in addition to</u> its function of protecting the distinct computing system. This feature is discussed in the Specification at, *e. g.*:

  page 33, lines 3 through 5,
  page 30, lines 16 through 21,
  page 36, lines 13 through 19,
  page 37, lines 17 through 21,
  page 38, lines 18 and 19,
  page 40, lines 8 through 12,
  page 41, lines 8 through 14;
  page 41, line 21, through page 42 line 2;
  page 42, lines 6 through 10,
  page 43, line 11, through page 48 line 4 (SUBSECTION 2[e])
  page 49, line 4, through page 50, line 19.

- Claims 33 and 65: protected system is COTS, "substantially exclusively" — This feature is discussed in the Specification at, *e. g.*, page 28, lines 14 through 16; page 29, lines 2 through 5 and 9 through 14; page 32, lines 2 through 7; and page 33, lines 13 through 15.

- Claim 33: protected system has a hardware subsystem for generating an error message (of that system) about incipient failure; network reacts to that message — The hardware subsystem recited here is not an element of the claimed invention (*cf.* claim 13 discussed above); however, the network and its circuits that react to the error message are elements of the claimed invention. This feature is inherent in the Specification at, *e. g.*, page 34, lines 13 and 14; page 35, lines 9 through 11, and continuing through line 22.

- Claim 50: network analyzes "inexactness" — In addition to comparing results from parallel channels (as discussed four "bullets" higher), the comparing portions of the network perform an algorithm to validate a match that is inexact; and in particular employs a degree of inexactness that is particularly suited to a type of computation under comparison. This feature is inherent in the Specification at, *e. g.*, page 52, lines 18 through 21 (considered together with reference 4, expressly incorporated at line 20); and page 54, lines 4 through 6.

- Claim 55: protected system has plural processors, at least one for running an application; and can generate a warning error message and respond to a recovery command — The protective-network circuits guard "any such system" from failure. The circuits identify and correct

failure of "any of such processors". See *e. g.*, page 30, lines 6 through 8, and page 55, lines 14 and 15 (also *e. g.*, page 52 lines 16 through 18, as well as page 32 lines 10 and 11). These passages make clear that the several protected processors can be parallel or mutually redundant.

- Claim 62: this claim and its dependent claims are <u>not</u> presented on appeal.

  (The Appellant respectfully asks permission to exclude these claims from the appeal; and — after the Appeal is concluded — to amend these six claims [62 through 64, and claims 76 through 78] to correct an accidental mis-wording. The last paragraph should be conformed to claim 55, lines 9 through 13. If the Board would prefer, however, the Appellant would be glad to cancel those claims without prejudice now.)

- Claim 65: protected system has subsystems for, respectively, generating a response of the system to incipient failure, and receiving recovery commands; network <u>interposes</u> analysis and corrective reaction between these subsystems — In other words, the protective network "inserts" between the two subsystems of the computing system (1) an interpretation of the protected system's "response to failure" and (2) generation of a recovery command. This feature is discussed in the Specification at, *e. g.*, page 34, lines 13 through 17; page 37, lines 12 through 17; and page 38, lines 15 and 16.

- Claim 81: an "M-node" (monitoring node, part of the protective network) waits for an error signal from the "C-node" (protected computing system) indicating incipi-

ent failure, and the M-node responds by sending a recovery command to the C-node. An "A-node" (adapter node, or terminals) transmits the error signal and recovery command between the C- and M-nodes. The M-node cannot, and does not, run any application program. These features are inherent in the Specification (and associated drawings) at, *e. g.*, page 34, lines 7 through 20; page 37, lines 12 through 17; and page 38, lines 6 through 10, and 15 and 16.

(8) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL Pages

- Claim 79 is rejected under 35 USC § 112, first paragraph (written-description requirement) — Specifically, the Examiner argues that the invention of claim 79 "is believed to be a result of a conversation [between the Examiner and the] Applicant, and as such was not held by the time of the filing of the disclosure."

  Applicant concurs that key subject matter ("a circuit breaker") of a negative limitation in claim 79 was first expressly introduced into this case by the Examiner in a telephone interview. This fact has been recounted in an interview summary, and remarks of later Amendments.

- Claims 2, 3, 7, 12, 19, 24, 27, 41, 54 and 61, and claims 65 through 69 are all rejected under 35 USC § 112, second paragraph (indefinite for failure to particularly point out and distinctly claim) — Examiner Bonzo argues that he is "unable to determine the bounds of" the phrase (underscore added) "substantially exclusively made up of substantially commercial, off-the-shelf components".

  His supervisor, Examiner Beausoliel, in a telephone interview conceded that the second occurrence of the word "substantially" (underscored above) had previously been removed by amendment, leaving only the first occurrence (not underscored above). Mr. Beausoliel, however, then argued (still on the phone) for indefiniteness of even the remaining phrase "substantially exclusively" alone.

- Claims 4, 16, 36, 47, 59, 63, 66 and 82 are rejected under 35 USC § 112, fourth paragraph (failure to further limit a parent claim) — Specifically, the Examiner takes the position that the protected computer system, first

recited in preamble of the parent claims, is necessarily an element of the claimed combination. The Examiner also writes that failure of that system, also first recited in parent-claim preamble, is also therefore necessarily an element of the claimed combination.

Given these arguments, the Examiner finds that in these dependent claims 4, 16 etc. the recitations intended to add the protected computer system into the claimed invention are necessarily "redundant limitations", violating the rule of 35 USC § 112, fourth paragraph.

- These claims are rejected under 35 USC § 102(b), as anticipated by U. S. 4,995,040 to David W. Best *et al.*:

  1
  4 through 8
  11
  13 through 17
  19, 20, 42, 44, 45, 47, 48, 53, 54 and 70.

- The claims listed below are rejected under 35 USC § 103, as obvious over the above-identified "Best" patent in view of a 1985 research paper written by the Applicant/Appellant in the present case, *The N-Version Approach to Fault-Tolerant Software* (hereinafter cited as "Avizienis '85").

  2, 3, 9, 10, 12 and 18
  21 through 24
  33 through 38
  41, 43, 46, 49, 50, 51, 52
  55 through 61
  65 through 69
  71, 75
  80 through 83

(9) ARGUMENTS Pages

Appellant submits the following principled reasoning, with respect to each ground of rejection presented in the preceding section "(8)", for consideration by the Board.

The undersigned notes that in the *Federal Register* the comments to the Board rules appear to favor "claim by claim" prosecution, and argument, rather than consolidation of claims for argument. The undersigned concurs in that preference, and will argue only a few claims grouped, but apologizes to the Board for the resulting considerable length of this section.

First a summary is given here in numerical order by claim number; then, starting at page 20, Appellant presents an analysis which begins in a more helpful order by main conceptual points:

claim(s) number	argued	SUB-SECTION	page
1, 5, 8, 10 and 11	as a group	1	20
2	separately	9a	28
3	separately	9b	29
4	separately	9c	29
5 (with 1, 8, 10 & 11)	as a group	1	20
6	separately	9e	29
7	separately	9f	30
8 (with 1, 5, 10 & 11)	as a group	1	20
9	separately	9g	30
10 & 11 (with 1, 5 & 8)	as a group	1	20
12	separately	9h	31
13, 14, 17, 20 & 22	as a group	9i	31
15	separately	9j	32
16	separately	9k	32
17 (with 13, 14, 20 & 22)	as a group	9i	31

claim(s) number	argued	SUB-SECTION	page
18	separately	9L*	33
19	separately	9m	33
20 (with 13, 14, 17 & 22)	as a group	9i	31
21	separately	9n	33
22 (with 13, 14, 17 & 20)	as a group	9i	31
23	separately	9o	34
24	separately	9p	35
25 through 32 [CANCELED]	~	~	~
33	separately	9q	35
34	separately	9r	36
35	separately	9s	36
36	separately	9t	37
37	separately	9u	37
38	separately	9v	38
39 and 40 [CANCELED]	~	~	~
41	separately	9w	38
42, 44, 45 and 53	as a group	9x	39
43	separately	9y	39
44 & 45 (with 42 & 53)	as a group	9x	39
46	separately	9z	40
47	separately	9aa	40
48	separately	9bb	40
49	separately	9cc	41
50 and 71	as a group	9dd	41
51	separately	9ee	42
52	separately	9ff	42
53 (with 42, 44 & 45)	as a group	9x	39
54	separately	9gg	42

*For clarity, lower-case "l" is presented as a capital, "L".

claim(s) number	argued	SUB-SECTION	page
55 and 57	as a group	2	20
56	separately	9hh	43
57 (with 55)	as a group	2	21
58	separately	9jj	44
59	separately	9kk	44
60 [CANCELED]	~	~	~
61	separately	9LL*	45
62 through 64, & 76 through 78 [NOT PRESENTED ON APPEAL; explanation at page 12.]			
65 and 67	as a group	4	22
66	separately	9mm	45
67 (with 65)	as a group	4	22
68	separately	9nn	46
69	separately	9oo	46
70	separately	9pp	47
71 (with 50)	as a group	9dd	41
72 [CANCELED]	~	~	~
73	separately	9qq	47
74	separately	9rr	48
75	separately	9ii	43
76 through 78 (with 62 through 64) [NOT PRESENTED ON APPEAL; explanation at pages 12 and 111.]			
79	separately	8	27
80	separately	9ss	48
81	separately	9tt	49
82	separately	9uu	50
83	separately	9vv	50

*For clarity, lower-case "l" is presented as a capital, "L".

ARGUMENTS, FIRST ORGANIZED BY CONCEPTUAL POINTS (through SUBSECTION 7, below):

1. Hardware — No cited art satisfies the claim-1 recitation of "a hardware network of components having substantially no software".

This point implicates claims 1 through 12; however, most of those claims also have additional recitations that are believed to confer patentability. Therefore the Appellant here presents the following reasoning with respect to only claims 1, 5, 8, 10 and 11, argued together as a group:

This limitation, "having substantially no software", clearly distinguishes the Best patent. Best's cited circuits are operated by associated software, most prominently avionics software. Please see the October 24, 2006 Request for Reconsideration (hereinafter "*October 2006 request*"), at page 2, and the May 15, 2006 Amendment in the section bridging pages 34 & 35 (hereinafter styled "*May ammt.* 34-35"), and the declaration of Jean-Claude Laprie at page 6, paragraph 24 (hereinafter "*Laprie* 6 ¶ 24"). As to rejection related to use of "Such", please see SUBSECTION 5 below.

Best expressly teaches dynamic software control over his circuits. More details appear in SUBSECTION 6 below (pages 24 and 25). Furthermore, his hardware does not protect operation of the avionics software in his associated computer system; rather, the software just runs the hardware.

(Claims 2 through 12 are taken up in later subsections.)

2. "Generic" infrastructure, capable of protecting virtually any computing system that can issue an error message and handle a recovery command — No cited art teaches this limitation.

This point implicates claims 3, 23, 35, 46, 69 and 74 — and in addition claims 55 through 59, and claim 75, although in these latter six claims the word "generic" does not appear. All of these claims, however, also contain other recitations

that are believed to confer patentability. Therefore the Appellant here presents the following reasoning with respect to only claims 55 and 57, argued as a group (the "generic" concept as defined is a prominent limitation of claim 55). The remaining enumerated claims are taken up in later subsections.

(1) The control software of Best is not generic. It is the opposite, *i. e.* entirely custom written to run his hardware. Therefore Best cannot protect "any system that can issue an error message and handle a recovery command". (Please see claim 55 lines 2 through 6, and lines 14 and 15.)

(2) In the DEDIX experiment (described in the cited Avizienis '85 paper), programs had to be custom written specifically with "cross-check" points. Whatever faults the DEDIX "handled" were all set by those cross-check points, *i. e.* by custom features of the programs. Appellant respectfully adds that these cross-check points were not "error messages" as recited in the subject limitation.

In support of these points, please see *October 2006 request* at page 3; *May ammt.* 57, section "(3)"; and *Laprie* 7-8 ¶¶ 27-28. (As to rejection related to use of "Such", please see SUBSECTION 5 below.)

3. Infrastructure guards against failure of an *entire* computing system — No cited art satisfies this limitation.

This point implicates claims 13 through 24, 34, 42 through 51, 53, 58, 70, 71, 73 and 74; however, once again, most of these claims also contain other recitations that are believed to confer patentability.

These claims just enumerated are taken up separately in later subsections.

Best never teaches guarding against failure of an entire computing system. His invention is expressly for "management, comparison, and correction of redundant digital data". He writes, "The present invention is a system for controlling and managing redundant inter-processor communication channels."

Such channels are much less than "an entire computing system". The fate of data after leaving his "host processor data bus" and flowing to the rest of Best's computing system is little concern of Best or his invention.

The Avizienis '85 paper likewise fails to teach guarding against failure of an entire computing system. This point, however, may be moot inasmuch as the combination of these two references is believed to be improper, as explained below (SUBSECTION 7). If the combination is indeed improper, then of course Avizienis '85 is not available for purposes of articulating a rejection.

Previous discussions of this point appear at *October 2006 request* at pages 3 and 4; *May ammt.* pages 41 and 42 (section titled "CLAIMS 13 THROUGH 17, AND 19 THROUGH 21"); and *Laprie* 11 ¶¶ 44-46. (As to rejection related to use of "Such", please see SUBSECTION 5 below.)

The Appellant also considers it significant, for purposes of distinguishing the art, that certain of these claims expressly recite that the apparatus is an "infrastructure". Although this term can be difficult to define precisely, the Appellant respectfully submits that Best's messaging circuits plainly do not serve as an infrastructure for guarding the entire associated host computer from failure — as does Appellant's disclosed and claimed invention.

4. "Substantially commercial, off-the-shelf" — In the Official Action of August 24, 2006, it is said that this phrase appears in the Applicant's claims. The associated rejections are confirmed in the Advisory Action of November 13, 2006. As shown below, all these rejections are believed to be factually in error.

The claims implicated by this point are claims 2, 3, 7, 12, 19, 24, 41, 54, 61, and 65 through 69; again, all these claims also contain other recitations that are believed to confer patentability. With this in mind, this present subsec-

tion 4 is directed to arguing only claims 65 and 67, argued together. The Appellant will argue all the others of these enumerated claims in later subsections.

These rejections, again, are factually in error. The questioned phrase was removed from the claims in the Amendment mailed October 12, 2005 — well over a year ago. Nevertheless the Examiners have refused to withdraw the rejection. Therefore the Appellant respectfully asks the Board to reverse all these rejections.

Appellant's most-recent comments on this point are in the November 22, 2006 Amendment at page 3, 2d paragraph; the *October 2006 request* at page 5, 2d and 3rd paragraphs; and the *May Ammt.* at pages 28 and 29. (As to rejection related to use of "Such", please see SUBSECTION 5 below.)

(The related phrase "substantially exclusively", if of interest to the Board, is discussed at page 15 (penultimate paragraph) above, as well as the paragraph bridging pages 11 and 12; and also in the November 22, 2006 Amendment at pages 1 through 5, and with reference to the exhibit accompanying that paper — and reproduced herein starting at page 76. The gravamen of those discussions is that this phrase is extremely common in issued patent claims, appearing in more than 400 patents during the last three decades.)

The basic limitation that the protected system is "substantially exclusively COTS" distinguishes the cited art, as both Best and the Avizienis '85 reference deal with distinctly customized systems. This point has been elaborated above (SUBSECTION 2) in the discussion of "generic" infrastructure.

5. "Such" — The specific usage of this term has been accepted by the Board in an earlier case, now 6,176,616 (column 20, lines 1, 4 and 44; column 22 line 7). It appears in a number of patents, most recently 7,156,482 (column 4, *e. g.* line 14).

In view of this broad prior acceptance, a categorical and *a priori* objection to this usage is believed to be error. In

fact, in some of the Official Actions in even the present case, this usage appears to be accepted.

This point implicates all of the claims, and Appellant asks that the Board overrule Examiner Bonzo's interpretations of this language, and their resulting contributions to all of his rejections. This request is with respect to only this single issue of the nomenclature using "such"; the Appellant of course does not otherwise wish to argue all the claims as a group.

Discussion of this point appears in *October 2006 Ammt.* at pages 6-7. Appellant respectfully adds that the claim-1 phrase "for deterring failure of a computing system" does not make the system part of the claimed combination — see, *e. g., Ex parte* Philippe Lemoine, Appeal 94-0216 (unpublished, December 27, 1994), paragraph bridging pages 12 and 13 (Appellant concedes that *Lemoine* is not precedential on this issue).

Also, "such" as a very specialized article (*i. e.*, substitute for "the") appears in the Patent Statute itself — 35 U.S.C. § 252, ¶ 2 (first two occurrences), quoted without adverse comment in at least one BPAI precedential opinion, namely *Eggert,* Appeal 2001-0790, 67 USPQ2d 1716 (May 29, 2003), at 15.

Of course every case is different from every other; but in view of (1) that precedent, coupled with (2) the Appellant's prerogative to be "his own lexicographer", and (3) the beneficial impact of this usage on the particularity and distinctness of the claims (discussed above at page 9), it is respectfully submitted that the Examiner's rejections are without authority.

6. The infrastructure is not controlled by any associated host computer that is capable of running any application program — No cited art satisfies this limitation.

This point implicates at least claims 38, 48 and 70. Since these claims all contain other limitations which even further enhance patentability, however, the Appellant presents

this reasoning here only for cross-reference from later subsections that argue these claims separately.

Appellant discussed related points in *October 2006 Ammt.* at pages 7-8.

Best teaches (column 6, lines 29 through 31) performing *e. g.* avionics computations in his associated machines. These would be software applications; therefore Best fails to satisfy this "no control by associated host that can run applications" limitation.

In the Official Action it is asserted that Best's circuits (page 11, paragraph 48, emphasis added):

> "are not controlled by any associated host computer that is capable of running any application program (Best does not disclose this type of host or control)."

Appellant begs to differ:

Best does expressly disclose one and preferably several host computers that are associated with and cooperate with his circuits. He also writes explicitly that the host or hosts exert control, and indeed apparently real-time control (column 3, lines 61 through 65, emphasis added):

> "[T]he global buses are dynamically grouped under software control to form redundant communication channels. Messages over these channels represent the computational results of the redundant computers interconnected by the network."

Even in the absence of these plain statements, it would be inherent that the associated host or hosts must "control" their messaging modules. From Best's disclosure taken as a whole, these messaging circuits are simply robot slaves that snap to attention to send and receive at the pleasure of the host or hosts.

7. Failure to show proper motivation for combination of references — The two prior-art citations are incompatible technologies, with no real motivation for combining. Also, they coexisted for ten years before Applicant's filing, but no other workers proposed their combination — additional basis for seeing absence of motivation.

This point implicates all claims rejected under § 103 and presented in this appeal, namely: claims 2, 3, 9, 10, 12, 18, 21 through 24, 33 through 38, 41, 43, 46, 49, 50, 51, 52, 55 through 61, and 65 through 69. Many of these claims also contain additional recitations that confer or enhance patentability; therefore the Appellant here presents this reasoning for cross-reference in later subsections that argue these enumerated claims separately.

Appellant's discussions appear *e. g.* at *May ammt.* 45-49, showing these known facts (to which the Official Actions make no substantive response):

- combination of the two references offers no real benefit, and so is not properly motivated (*May ammt.* 48-49; *Laprie* 8-9 ¶¶ 30-36 and 9-10 ¶¶ 38-40);
- the references describe technologies that would work together poorly, and that skilled artisans do not regard as "going together" (*Laprie* 16, ¶ 68);
- if combination of the references were obvious, that combination would have been invented by others (*May ammt.* 45-46);
- this reasoning is approved by the High Courts (*May ammt.* 47);
- obviously there has been continuing strong need (*May ammt.* 46-47); and
- for certain claims, neither reference "even satisfies . . . the underlying independent claim" (*Laprie* 6 ¶ 24, and *e. g.* 11 ¶¶ 43-50).

As to the Laprie Declaration, cited above at several points, the Appellant wishes to point out that Dr. Laprie does not purport to be an expert in the field of patents — but, as he himself expressly observes in his paragraphs 33 through 36 (pages 8 and 9), he is excellently qualified to testify on the issue of obviousness to a skilled person in the art.

8. Negative limitation of claim 79, argued separately — In a phone interview with the Appellant Dr. Avizienis, and the undersigned, the Examiner said the invention defined in the all-hardware claims "could be a circuit breaker". Appellant does not agree that any of the claims defines a circuit breaker.

The Appellant, however, certainly knew since before filing this case that the invention was not a circuit breaker. The Appellant also respectfully submits that the Specification as originally filed, taken in its entirety, makes clear that the invention is in fact not a circuit breaker — even though, as the Examiner observes, the original Specification does not use the words "circuit breaker". In other words, this fact is inherent in the Specification.

(Hence, since the Appellant's "possession" of the claimed invention does not seem to be seriously in doubt, Appellant would be glad to add the language of claim 79 into the Specification — if that would be helpful to the formalities of Section 112, first paragraph,"written-description requirement".)

Appellant submits that the Examiner's statement on the phone — taken together with Appellant's later account of the interview, and the Examiner's own account of it — constitutes a citation of prior art: "a circuit breaker". It is of record that the Examiner made such a citation, orally.

When art is cited on the record, the Appellant is entitled to draft a claim to appropriately distinguish that art. In doing so, the Appellant is not limited to what appears verbatim in the Specification, but is plainly entitled to draw

upon what is inherent in the Specification. In this situation the Appellant believes that he is entitled to simply state what the invention is not; and he has done so in claim 79.

Much of this reasoning appears in the file wrapper in *e. g.*, the Supplemental paper of October 27, 2005, page 24; and the Amendment of May 15, 2006, pages 40 and 41. (As to rejection related to use of "Such", please see SUBSECTION 5 above.)

9. Individual claims argued — All claims discussed are argued separately — EXCEPT in subsections:

1 (claims 1, 5, 8, 10 and 11, argued together),
2 (claims 55 and 57, argued together),
4 (claims 65 and 67, argued together)
9i (claims 13, 14, 17, 20 and 22, argued together),
9x (claims 42, 44, 45 and 53, argued together), and
9dd (claims 50 and 71, argued together).

(In the remainder of this SUBSECTION 9, the prefix "9" is suppressed, except in cross-references, where it is retained for clarity. Thus for example, the first SUBSECTION "a. Claim 2" below is identified in cross-references as "SUBSECTION 9a" — as in, also the numerical summary that starts on page 17 above.)

a. Claim 2 — In addition to the "all hardware" limitations of base-claim 1 (SUBSECTION 1 above), claim 2 is believed to be even more strongly patentable by virtue of these additional reasons, in combination:

- claim 2 recites that the protected system is "substantially exclusively COTS" (SUBSECTION 4 above) — not found in the currently cited art since the protected systems (if such there be) in Best and Avizienis '85 are both custom systems; and
- the references are believed to be improperly combined (SUBSECTION 7 above).

(As to rejection related to use of "Such", please see SUBSECTION 5 above.)

b. Claim 3 — In addition to the "all hardware" limitations of base-claim 1 (SUBSECTION 1 above), claim 3 is believed to be even more strongly patentable by virtue of these additional reasons, in combination:

- claim 3 recites an infrastructure, which is believed to be absent from the cited art — as mentioned for claim 81 above (SUBSECTION 6);
- claim 3 recites that the infrastructure is "generic" in the stated sense presented above (SUBSECTION 2); and
- the references are believed to be improperly combined (SUBSECTION 7 above).

(As to rejection related to use of "Such", please see SUBSECTION 5 above.)

c. Claim 4 — In addition to the "all hardware" limitation of base-claim 1 (SUBSECTION 1 above), claim 4 is believed to be even more strongly patentable because it defines an expanded combination that adds the protected computing system.

As previously noted, Appellant of course would be glad to present claim 4 in independent form, if that would be met with favor. Presumably that would obviate any theoretical objection based on the "further limiting" requirement. (As to rejection related to use of "Such", please see SUBSECTION 5 above.)

d. Claim 5 — argued above, with claim 1 (SUBSECTION 1).

e. Claim 6 — In addition to the "all hardware" limitations of base-claim 1 (SUBSECTION 1 above), claim 6 is believed to be even more strongly patentable by virtue of these further reasons:

- claim 6 says the protected circuits are "not capable of running any application program" — closely related to limitations discussed in SUBSECTION 6 above;
- although Best may teach circuit portions to detect and correct for failure, he makes explicit that his circuits are controlled by software, such as the "avionics" software that he mentions and the Examiner has noted — helpful to Best's purposes, as the software system is typically programmed to recognize what reasonable avionics communications look like.

(As to rejection related to use of "Such", please see SUBSECTION 5 above.)

f. Claim 7 — Besides the "all hardware" limitations of base-claim 1 (SUBSECTION 1 above), claim 7 is even more strongly patentable by virtue of these further reasons:

- claim 7 recites the "substantially-exclusively" COTS limitation that is also discussed above (SUBSECTION 9a) for claim 2; and
- the Examiner's argument in the current Action (page 6, paragraph 7) is not understood, but in any event seems to miss the point that it is the software, in the hosts, that is in control of the hardware — not vice versa (column 3, lines 61 through 63).

(As to rejection related to use of "Such", please see SUBSECTION 5 above.)

g. Claim 9 — In addition to the "all hardware" limitation of parent claims 1 and 8 (SUBSECTION 1 above, page 20), claim 9 is believed to be even more strongly patentable in view of these additional reasons:

- its recitation that the parallel computing channels are "of diverse design or manufacture"; and

- the references are believed to be improperly combined (SUBSECTION 7 above).

The Official Action attempts to implicitly amend the phrase "of diverse design or origin" to read instead merely "generated at a diverse origin" — in other words, to cover generation of messages sent from different sending people or sending machines. Applicant's claim, however, addresses "channels" (equipment, apparatus) that is of diverse design, or comes from diverse factories etc.

With these corrected understandings, the cited art cannot meet this limitation. (As to rejection related to use of "Such", please see SUBSECTION 5 above.)

h. Claim 12 — Besides the "all hardware" limitations of base-claim 1 (SUBSECTION 1 above), claim 12 is believed to be even more strongly patentable because of:

- the "substantially-exclusively" COTS limitation that is also discussed above (SUBSECTION 9a) for claim 2;
- its recitation of "interposing analysis and a corrective reaction" between subsystems of the protected computing system; and
- the references are believed to be improperly combined (SUBSECTION 7 above).

Appellant believes that the two recitations just mentioned are absent from the cited art. (As to rejection related to use of "Such", please see SUBSECTION 5 above.)

i. Claims 13, 14, 17, 20 and 22, argued together — These claims are believed to be patentable over the art by virtue of these two recited limitations in claim 13:

- the apparatus claimed can deter failure of an *entire* computing system (the Appellant submits that, as

pointed out in SUBSECTION 3 above, no cited art teaches such protection; and

- besides this protection against failure of the entire computing system, the invention of claims 13 and 14 also protects its own circuits from failure.

Please note, these are two distinct layers of protection. The art is not seen to teach any such combination. (SUBSECTION 5 above discusses rejection due to use of "Such".)

j. Claim 15 — Besides the "entire system" and self-protection limitations of base-claim 13 (SUBSECTION 9i, immediately above), claim 15 is even more strongly patentable by virtue of its recitation of an "infrastructure".

As noted above (SUBSECTION 6), no infrastructure is taught in the cited art. The Examiner has not supported his assertion (Office Action at page 8, column 15) that "the network is an infrastructure". (SUBSECTION 5 above discusses rejection due to use of "Such".)

k. Claim 16 — In addition to the "entire system" limitations of base-claim 13 (SUBSECTION 9i above), claim 16 is believed to be even more strongly patentable by virtue of its expansion of the claimed combination to incorporate the protected computing system.

No such combination is found in the art now cited. It appears that rejection of claim 16 (as well as claim 4) flows primarily or only from the Examiner's belief that incorporation of the protected system is a "redundant limitation" — and therefore that dependent claim 16 does not "further limit" the parent claim.

That theory is believed to be incorrect — as discussed at length above, under the heading "Such" (SUBSECTION 5). Appellant submits that that ground of rejection

has there been shown to be not authorized by the Patent Statute.

l. Claim 18 — Besides the "entire computing system" limitations of base-claim 13 (SUBSECTION 9i above), claim 18 is even more strongly patentable because:

- claim 18 is limited to circuits that "receive error messages warning of incipient such failure, and issue recovery commands to the system" (which, as the Examiner appears to concede, are not found in Best — rather, his invention reacts to detected errors directly without error "messages" *per se*); and
- the references are believed to be improperly combined (SUBSECTION 7 above) — so that the cited Avizienis '85 paper is not available to complete the claimed combination. (SUBSECTION 5 above discusses rejection due to use of "Such".)

m. Claim 19 — In addition to the "entire computing system" limitations of base-claim 13 (SUBSECTION 9i above), claim 19 is believed to be even more strongly patentable by virtue of its "substantially-exclusively COTS" limitation that is also discussed above (SUBSECTION 9a) for claim 2, and (as there shown) not met by the now-cited art. (SUBSECTION 5 above discusses rejection due to use of "Such".)

n. Claim 21 — In addition to the "entire system" and self-protection limitations of base-claim 13 (SUBSECTION 9i above), claim 21 is believed to be even more strongly patentable in view of these additional reasons:

- its recitation that the parallel computing channels are "of diverse design" (*cf.* discussion of claim 9, in SUBSECTION 9g above); and

- the references are believed to be improperly combined (SUBSECTION 7 above).

Here too, analogously to the rejection of claim 9, the Official Action shifts the phrase "of diverse design" to the diluted form "generated at a diverse origin" — in other words, to cover generation of messages that come from different sending people or machines. Applicant's claim, however, addresses channels (*i. e.*, equipment) that is of diverse design etc.

The rejection of claim 21 seems to start on a § 102 theory (first four lines of paragraph 21, on page 24) but then segues to § 103. To cover both of these positions in the Action:

- the analysis of the "diverse design" limitation stated in the second paragraph on this page shows that the cited art cannot meet this limitation under § 102; but, above that, on this page
- the bulleted paragraph deals with § 103: as the proposed combination of references is believed to be improper (SUBSECTION 7), Avizienis '85 (page 1500) is not available to complete the § 103 rejection.

(SUBSECTION 5 discusses rejection due to use of "Such".)

o. Claim 23 — This claim, like claims 55 and 15 (SUBSECTIONS 2 and 9j), recites an infrastructure, not taught in the art — but claim 23 (like 55) goes further than claim 15, saying that the infrastructure is "generic in that it can accommodate any such system that can issue an error message and handle a recovery command." This claim is believed to be patentable because, in addition to the features of base-claim 13 (SUBSECTION 9i above):

- as explained at length earlier (*e. g.* SUBSECTIONS 2 and 9j above), none of the cited art teaches an

infrastructure or any failure-deterring apparatus that is "generic" in the stated sense — rather, the cited references both teach highly custom systems; and

- the references are believed to be improperly combined (SUBSECTION 7 above) — and therefore the cited Avizienis '85 paper is not available to complete the combination of references proposed by the Examiner.

(SUBSECTION 5 discusses rejection due to use of "Such".)

p. Claim 24 — Besidesthe "entire computing system" limitations of base-claim 13 (SUBSECTION 9i above), claim 24 is believed to be even more strongly patentable because of:

- its "substantially-exclusively COTS" limitation that is also discussed above (SUBSECTION 9a) for claim 2, and (as there shown) believed not to be met by the cited art;
- its recitation of circuits that interpose "analysis and a corrective reaction" between two subsystems of the protected computing system, also not met by the cited art; and
- also, the references are believed to be improperly combined (SUBSECTION 7 above) — and therefore the cited Avizienis '85 paper is not available to complete the combination of references the Examiner proposes.

Although claim 24 is thus in these regards analogous to claim 12, these two claims differ by depending from, respectively, claims 1 and 13. (SUBSECTION 5 discusses rejection due to use of "Such".)

q. Claim 33 — This claim is believed to be patentable by virtue of these reasons, in combination:

- claim 33 recites that the protected system is "substantially exclusively COTS" (SUBSECTION 4 above) — not found in the currently cited art since the protected systems (if such there be) in Best and Avizienis '85 are both custom systems;
- the references are believed to be improperly combined (SUBSECTION 7 above) — hence Avizienis '85 is not available to complete the combination of references as proposed in the Official Action; and
- this claim recites protective circuits that react to an error message about incipient failure, from a hardware subsystem of the protected system; and the Official Action (pages 29 and 30) concedes that Best alone fails to "expressly" teach these features.

(SUBSECTION 5 discusses rejection due to use of "Such".)

r. Claim 34 — As detailed earlier (SUBSECTION 3), Best cannot meet the limitation that the invention guards the "entire" computing system from failure. This limitation is in addition to the above-stated three reasons for patentability of the base-claim 33.

The "entire system" limitation is moreover strengthened by the recitation that this guarding is "in response to" the above-mentioned "error message" (generated by the protected system) — which the Official Action (page 30) also concedes Best does not disclose "explicitly". (SUBSECTION 5 discusses rejection due to use of "Such".)

s. Claim 35 — The cited art fails to meet the recitation that the network is generic in the specified sense: it can accommodate any such system that can issue an error message and handle a recovery command. The reason, set forth earlier (SUBSECTION 2), is that Best and Avizienis '85 are both highly custom systems, not at all generic.

Furthermore, Appellant submits that Avizienis '85 is not available to contribute to the present Section-103 rejection of this claim — because as shown above (SUBSECTION 7) the references are combined improperly. (SUBSECTION 5 discusses rejection due to use of "Such".)

t. Claim 36 — In addition to the "COTS" limitation of base-claim 33 (and improper combination of the references in rejecting that claim), claim 36 is believed to be even more strongly patentable by virtue of its expansion of the claimed combination to incorporate the protected computing system.

As detailed earlier (SUBSECTIONS 5 and 9k above), such protection is not found in the cited art. Therefore it appears that rejection of claim 36 (as well as claims 4, 36 etc.) flows primarily or only from the Examiner's belief that incorporation of the protected system is a "redundant limitation" — and therefore that dependent claim 16 does not "further limit" the parent claim.

That theory is believed to be incorrect — as shown at length above, under the heading "Such" (SUBSECTION 5). Appellant submits that that ground of rejection has there been shown to be not authorized by the Patent Statute.

By rejecting claim 36 under Section 103 (at page 32 of the Official Action), the Examiner appears to concede that Best alone is not sufficient; however, Appellant has shown above (SUBSECTION 7) that the two references are combined improperly. Avizienis '85 is therefore inapposite.

u. Claim 37 — In addition to the "COTS" limitation of base-claim 33 (SUBSECTIONS 4, 7 and 9q above), and in addition to inclusion of the protected system in the claimed combination of parent claim 36 (SUBSECTION 9t above), claim 37

is believed to be even more strongly patentable in view of these additional reasons:

- its recitation that the parallel computing channels are "of diverse design or manufacture"; and
- the references are believed to be improperly combined (SUBSECTION 7 above).

The Official Action, as noted earlier, implicitly weakens the phrase "of diverse design or origin" to read instead merely "generated at a diverse origin" — thus covering generation of messages merely sent from different sending people or machines. Applicant's claim, however, addresses apparatus ("channels" are apparatus) that is of diverse design or comes from diverse factories etc.

Given these corrected understandings, the cited art cannot meet this limitation. (SUBSECTION 5 discusses rejection due to use of "Such".)

v. Claim 38 — In addition to the above-discussed "COTS" limitation in the base-claim, claim 38 is believed to be *a fortiore* patentable because:

- the cited art cannot meet the limitation "not controlled by any associated host computer that is capable of running any application program" (Appellant provided details above, SUBSECTION 6); and
- the references are believed to be improperly combined (SUBSECTION 7 above) — so that Avizienis '85 is not available to complete the combination of references upon which the Examiner relies.

(SUBSECTION 5 discusses rejection due to use of "Such".)

w. Claim 41 — In addition to the above-noted "COTS" limitation, claim 41 is believed to be more strongly patentable because:

- the cited art cannot meet the limitation that the protective circuits interpose analysis and a corrective action between a response-generating unit in the protected computing system — which has generated an error message from that protected system — and a command-receiving unit in that system; and
- the references are believed to be improperly combined (SUBSECTION 7 above).

As to the first of these points, it is respectfully noted that Best, although he may provide corrective reaction to an existing condition, does not teach generation of an "error message" — as evidently conceded by the Examiner (page 34, paragraph 41). In view of the second of these points, Avizienis '85 is not available to complete the proposed combination of references. (SUBSECTION 5 discusses rejection due to use of "Such".)

x. Claims 42, 44, 45 and 53, argued together — As detailed earlier (SUBSECTION 3), Best cannot meet the limitation that the invention guards the "entire" computing system from failure. (SUBSECTION 5 discusses rejection due to use of "Such".)

y. Claim 43 — In addition to the above reasons for patentability of base-claim 42, this dependent claim 43 is further believed to be patentable because:

- cited art cannot meet the "diverse design or origin" limitation, as shown in *e. g.* SUBSECTION 9u; and
- as also noted earlier (SUBSECTION 7), the references upon which the Examiner relies here are combined improperly — and the reliance upon Avizienis '85 should not be permitted.

(SUBSECTION 5 discusses rejection due to use of "Such".)

z. Claim 46 — In addition to the above reasons for patentability of base-claim 42, this dependent claim 46 is further believed to be patentable because:

- cited art cannot meet the "generic" (as defined) limitation, as shown in *e. g.*, SUBSECTION 2; and
- as also detailed earlier (SUBSECTION 7), the references upon which the Examiner relies here are combined improperly; hence Avizienis '85 is not available to complete the Examiner's contentions.

(SUBSECTION 5 discusses rejection due to use of "Such".)

aa. Claim 47 — In addition to the "entire system" limitations of base-claim 42 (SUBSECTION 9i above), claim 47 is believed to be even more strongly patentable by virtue of its "narrowing" expansion of the claimed combination to encompass the protected computing system.

Appellant submits that no such combination is found in the art now cited. Therefore it appears that rejection of claim 47 (as well as claims 4 and 16 etc.) flows primarily or only from the Examiner's belief that incorporation of the protected system is a "redundant limitation" — and therefore that dependent claim 47 does not "further limit" the parent claim.

That theory is believed to be incorrect — as discussed at length above, under the heading "Such" (SUBSECTION 5). Appellant submits that that ground of rejection has there been shown to be not authorized by the Patent Statute.

bb. Claim 48 — In addition to the above-discussed "entire system" limitation in the base-claim 42, claim 48 is believed to be even more plainly patentable because:

- the cited art cannot meet the limitation "not controlled by any associated host computer that is capable of running any application program" (in support of this plain fact, Appellant has provided Best's express, detailed statements — above at SUBSECTION 6); and
- the references are believed to be improperly combined (SUBSECTION 7 above) — so that Avizienis '85 is not available to complete the combination of references upon which the Examiner relies.

cc. Claim 49 — In this claim the "entire system" limitation of base-claim 42 is strengthened by the recitation that this guarding is in reaction to an "error message" produced by the protected system. The Official Action, although in discussion of a different claim (claim 33, pages 29 and 30), concedes in so many words that Best does not disclose "explicitly" this "error message" feature.

Protective capabilities of a system that responds to error messages from a protected system differ from those of a system that detects error circumstances directly.

Also, Appellant has shown (SUBSECTION 7 above) that the cited references cannot be properly combined, in support of any such rejection. Accordingly it is believed that the rejection of claim 49 is improper.

dd. Claims 50 and 71, argued together — As detailed earlier (SUBSECTION 3), Best cannot meet the claim-50 limitation of deterring failure of the "entire" computing system. Claim 50, however, is even more clearly patentable because — as evidently conceded in the Official Action (page 42) — Best teaches nothing about inexact matching, particularly not any "degree of inexactness".

Since the Appellant has shown (SUBSECTION 7 above) that the cited references cannot be properly combined — in support of any such rejection — the Avizienis '85 reference (even if it does treat "inexactness") is not available to the Examiner as regards claim 50. It is thus submitted that rejection of claim 50 is improper.

ee. Claim 51 — In addition to the above-noted "entire system" recitation of base-claim 50, and to the earlier-detailed impropriety of the combination of references, this dependent claim goes on to an even more remote recitation (selection of a degree of inexactness, based on type of computation) that Best cannot meet — and Avizienis '85 is believed to be unavailable to meet.

ff. Claim 52 — In addition to the "entire system" recitation of base-claim 42, this dependent claim 52 introduces the limitation "plural processors" and circuit portions for identifying and correcting their failure. The Official Action (page 39, paragraph 52) appears to acknowledge this gap, and relies upon Avizienis '85 to fill it.

Appellant submits that the latter reference (even if it could fill it) is unavailable, because the references are (as shown in SUBSECTION 7 above) combined improperly.

gg. Claim 54 — This claim is believed to be patentable by virtue of these reasons, in combination:

- its recitation that the protected system is "substantially exclusively COTS" (SUBSECTION 4 above) — not found in the currently cited art since the protected systems (if such there be) in Best and Avizienis '85 are both custom systems;

- the reasons for patentability of the base-claim 42, as stated above at SUBSECTION 3 (and 9x); and
- impropriety of the combination of references (SUBSECTION 7 above) — because of which Avizienis '85 is not available to complete the combination of references as proposed in the Official Action

hh. Claim 56 — In addition to the reasons stated earlier (SUBSECTION 2) for patentability of base-claim 55, this dependent claim 56 recites that the "identifying portions" of the invention have "a section that corrects for" identified failure "by taking a processor out of operation". The Official Action relies upon Avizienis '85 for this limitation; however, as shown earlier (SUBSECTION 7 above) this reliance is believed to be improper because the combination of references itself is improper.

ii. Claim 75 — In addition to the reasons stated above (SUBSECTION 2) for patentability of base-claim 55:

- claim 75 includes a recitation that the protective circuits issue a recovery command; and when read together with the preamble of that parent claim 55, this recitation intimates that the recovery command is in response to an "error message" from the protected computing system, "warning of incipient failure"; and
- as respectfully submitted by the Appellant, impropriety in the combination of references leaves Avizienis '85 unavailable to complete the rejection planned by the Examiner.

The combined recitation of claims 55 and 75, just described here, distinguishes the art — because Best's cir-

cuits attempt to correct errors without receiving "an error message" as such.

jj. Claim 58 — In addition to the reasons just stated for parent claim 75, claim 58 further distinguishes the art by virtue of the additional recitation that the protective circuits protect the *entire* computing system. Contrary to the assertion in the Official Action (page 48, paragraph 58), Appellant has shown earlier (SUBSECTION 3, above) that no cited art teaches protecting an "entire" computing system.

kk. Claim 59 — In addition to the reasons stated above (SUBSECTION 9ii) for patentability of parent claim 75, claim 59 further distinguishes the art by virtue of incorporating the protected computing system.

As detailed earlier (*e. g.* SUBSECTION 9k above), such protection is not found in the art now cited. Therefore it appears that rejection of claim 59 (as well as claims 4, 36 etc.) flows from the Examiner's contention that incorporation of the protected system is a "redundant limitation" — and therefore that dependent claim 59 does not "further limit" the parent claim.

Appellant submits that that theory is incorrect, as set forth in detail above — under the heading "Such" (SUBSECTION 5). Appellant submits that the subject ground of rejection is there shown to be without authority under the Patent Statute.

By rejecting claim 36 under Section 103 (at page 32 of the Official Action), the Examiner appears to concede that Best alone is not sufficient; however, Appellant has shown above (SUBSECTION 7) that the two references are combined improperly.

ll. Claim 61 — In addition to the reasons stated above (SUBSECTION 9ii) for patentability of parent claim 75:

- claim 59 further distinguishes the art by reciting the "substantially exclusively COTS" limitation — as explained earlier (SUBSECTION 2); and
- the rejection asserted in the Official Action relies upon combination of Best with Avizienis '85, which as analyzed above (SUBSECTION 7) is an improper combination.

mm. Claim 66 — In addition to the reasons set forth earlier (SUBSECTION 4) for allowance of base-claim 65, Appellant submits that claim 66 is *a fortiore* allowable because it incorporates the protected system into the claimed combination, thus narrowing the claim.

Appellant respectfully reiterates his principled analysis that the line of reasoning adopted in the Official Actions (*i. e.* proposing that this dependent claim is faulty because it fails to "further limit" the base claim 65) is incorrect. As set forth earlier (INTRODUCTION, part b, at page 8; and SUBSECTION 5):

- the claimed combination of the parent claims expressly excludes the protected computing system; while
- the claimed combination of the dependent claims is expressly enlarged to include that protected system; the wording of these claims, however, is selected to avoid inconsistency with the parent claims.

It appears that the same effect could be obtained, though at somewhat greater cost, by writing all these dependent claims in independent form.

nn. Claim 68 — In addition to the reasons set forth earlier (SUBSECTION 4) for allowance of base-claim 65, Appellant submits that claim 68 is *a fortiore* allowable because:

- it further distinguishes the art by reciting that the protective circuits, "by responding to an error signal from such system, . . . protect the entire such system from failure";
- the rejection of claim 68 as well as its base-claim is based upon a combination of references that has earlier (SUBSECTION 7) been shown to be improper.

The reference here to an "entire" system simply continues the corresponding limitation in the base-claim 65. The fact that this protection is accomplished in response to an "error signal from such system", however, goes beyond the base claim.

As pointed out earlier (SUBSECTION 4), Best's reaction to failure circumstances is direct; it involves no such "error signal", as such, from the protected computing system. Hence the recitation of an error signal from the protected system does distinguish the cited art.

oo. Claim 69 — In addition to the reasons set forth earlier (SUBSECTION 4) for allowance of base-claim 65, Appellant submits that claim 69 is even more strongly patentable because:

- it further distinguishes the art by reciting that the protective apparatus is an infrastructure;
- it also distinguishes the art by reciting that the protected apparatus is "generic" in the defined sense — and, as noted earlier, neither Best nor Avizienis '85 discloses generic protected systems;

to the contrary, both are highly "custom" equipment; and

- claim 69 is rejected under Section 103, based on a combination of references that is believed to be improper, as detailed earlier (SUBSECTION 7).

pp. Claim 70 — In addition to the above-discussed reasons for patentability of the base-claim 13 (SUBSECTION 3 details the inability of the cited art to meet the "entire system" limitation in that claim, and SUBSECTION 9i notes as well the self-checking and -correcting provisions, lines 9 through 13 in that base-claim), claim 70 is believed to be even more plainly patentable because:

- the cited art cannot meet the limitation "not controlled by any associated host computer that is capable of running any application program" (in support of this plain fact, Appellant has provided Best's express, detailed statements — above at SUBSECTION 6); and
- the references are believed to be improperly combined (SUBSECTION 7 above) — so that Avizienis '85 is not available to complete the combination of references upon which the Examiner relies.

qq. Claim 73 — In addition to the reasons stated above for patentability of base-claim 50 (SUBSECTIONS 2 and 9dd show that Best does not deter failure of the "entire" computing system, and he also teaches nothing about "inexact-match" validation):

- claim 73 includes a recitation that the protective circuits guard the entire system by receiving "error messages" from the protected system, "warning of incipient failure" — and also issue "recovery com-

mands" to that system — whereas, as noted earlier (SUBSECTIONS 4 and 9cc), Best's circuits are believed to instead react directly to conditions, with no error message as such; and

- as respectfully submitted by the Appellant, impropriety in the combination of references leaves Avizienis '85 unavailable to complete the rejection planned by the Examiner.

For these several reasons, claim 73 distinguishes the art.

rr. Claim 74 — In addition to the reasons stated above for patentability of base-claim 50 (SUBSECTIONS 2 and 9dd show that Best does not deter failure of the "entire" computing system, and he also teaches nothing about "inexact-match" validation), claim 74 is *a fortiore* patentable because:

- it further distinguishes the art by reciting that the protective apparatus is an infrastructure;
- it distinguishes the art even more particularly by reciting that the protected apparatus is "generic" in the defined sense — and, as noted earlier, neither Best nor Avizienis '85 discloses generic protected systems; to the contrary, both are highly "custom" equipment; and
- claim 74 is rejected under Section 103, based on a combination of references that is believed to be improper, as detailed earlier (SUBSECTION 7).

ss. Claim 80 — In addition to the reasons stated above for patentability of base-claim 1 (SUBSECTION 1 points out that

the cited prior art all has associated software), claim 80 is even more strongly patentable because:

- it further distinguishes the art by reciting that the protective apparatus is connected to receive an "error signal" from the protected system, "in event of incipient failure" — and that this error signal causes the protective apparatus to provide a recovery signal to the protected system — whereas, as noted earlier (SUBSECTIONS 4, 9cc and 9pp), Best's circuits are believed to instead depend on reacting to detected conditions directly, without any error message (or "signal") as such; and
- as respectfully submitted by the Appellant (SUBSECTION 7), impropriety in the combination of references leaves Avizienis '85 unavailable to complete the rejection planned by the Examiner.

For all these reasons, claim 80 distinguishes the art.

tt. Claim 81 — This claim distinguishes the cited prior art because it recites that:

- the claimed invention is an "infrastructure" (also detailed in SUBSECTION 1), and
- a part of the infrastructure monitors the protected computing system (so-called C-node) "by waiting for an error signal, indicating incipient such failure, from" the protected system.

The capability of the latter limitation to distinguish the Best patent is discussed briefly in the preceding SUBSECTION 9ss, as well as more fully in earlier SUBSECTIONS 4 and 9pp.

uu. Claim 82 — In addition to the above-stated reasons for allowance of base-claim 81, the Appellant submits that claim 82 is *a fortiore* allowable because it incorporates the protected system into the claimed combination, thus narrowing the claim.

Appellant respectfully asserts once again that the line of reasoning adopted in the Official Actions (*i. e.* proposing that this dependent claim is faulty because it fails to "further limit" the base claim 65) is incorrect as a matter of principle. This point is set forth earlier (INTRODUCTION, part b, at page 8; and SUBSECTION 5, as well as *e. g. SUBSECTION* 9mm).

vv. Claim 83 — In addition to the above-stated reasons for allowance of base-claim 81, the Appellant submits that claim 82 *a fortiore* distinguishes the art because:

- the Official Action appears to concede (page 57, paragraph 82) that Best fails to teach the claimed "decision making node (D-node) for comparing output data generated by such plural C-nodes and reporting to the . . . M-node any discrepancy); and
- the Action goes on to rely upon the Avizienis '85 reference, which Appellant submits should be excluded, since the claim stands rejected over a combination of references that is improper (SUBSECTION 7).

(10) CLAIMS APPENDIX Pages

Following are all the claims in this case. The one allowed claim, claim 84, is included for the Board's convenience and for completeness.

For the Board's information, the date of most-recent amendment is included for each claim, other than the original claims.

1. (amended May 15, 2006) Apparatus for deterring failure of a computing system; said apparatus comprising:

a hardware network of components, having substantially no software and substantially no firmware except programs held in an unalterable read-only memory;

terminals of the network for connection to such system; and

fabrication-preprogrammed hardware circuits of the network for guarding such system from such failure.

2. (amended May 15, 2006) The apparatus of claim 1, particularly for use with such system that is substantially exclusively made up of commercial, off-the-shelf components; and wherein:

at least one of the network terminals is connected to receive at least one error signal generated by such system in event of incipient such failure of such system;

at least one of the network terminals is connected to provide at least one recovery signal to such system upon receipt of the error signal; and

the apparatus further comprises means for automatically responding to the at least one error signal by generating the at least one recovery signal for guarding all of such system against such failure.

3. (amended October 12, 2005) The apparatus of claim 1, wherein:

the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and handle a recovery command.

4. (original) The apparatus of claim 1, further comprising:

such computing system.

5. (original) The apparatus of claim 1, wherein:

the circuits comprise portions for identifying failure of any of the circuits and correcting for the identified failure.

6. (amended October 12, 2005) The apparatus of claim 1, wherein:

the circuits are not capable of running any application program.

7. (amended May 15, 2006) The apparatus of claim 1, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one hardware subsystem for generating a response of the system to failure; and wherein:

the circuits comprise portions for reacting to such response of such hardware subsystem.

8. (original) The apparatus of claim 1, particularly for use with a computing system that has plural generally parallel computing channels; and wherein:

the circuits comprise portions for comparing computational results from such parallel channels.

9. (amended May 15, 2006) The apparatus of claim 8, wherein:

the parallel channels of such computing system are of diverse design or manufacture.

10. (amended May 15, 2006) The apparatus of claim 1, particularly for use with a computing system that has plural processors; and wherein:

the circuits comprise portions for identifying such failure of any of such processors and correcting for identified such failure.

11. (amended October 12, 2005) The apparatus of claim 1, wherein:

the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising:

at least three data-collecting and -responding modules, and

processing sections for conferring among the modules to determine whether any of the modules has failed.

12. (amended May 15, 2006) The apparatus of claim 1, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; and wherein:

the circuits comprise portions for interposing analysis and a corrective reaction between such response-generating subsystem and such command-receiving subsystem.

13. (amended May 15, 2006) Apparatus for deterring failure of an entire computing system, wherein the computing system optionally includes plural mutually redundant modules; said apparatus comprising:

a network of components having terminals for connection to such system, wherein the network is constructed to be initially and permanently distinct from such computing system including all of such redundant modules if present; and

circuits of the network for operating programs to guard such entire system from such failure;

the circuits comprising portions for identifying such failure of any of the circuits and correcting for the identified such failure.

14. (amended May 15, 2006) The apparatus of claim 13, wherein:

the program-operating portions comprise a section that corrects for the identified such failure by automatically taking a failed circuit out of operation.

15. (amended October 12, 2005) The apparatus of claim 13, wherein:

the network is an infrastructure that continuously waits to respond to messages from such system.

16. (original) The apparatus of claim 13, further comprising:

such computing system.

17. (amended May 15, 2006) The apparatus of claim 13, wherein:

the program-operating portions comprise at least three of the circuits; and

such failure is identified at least in part by majority vote among the at least three circuits.

18. (amended May 15, 2006) The apparatus of claim 13, wherein:

to guard such entire system from failure, said circuits receive from such system error messages warning of incipient such failure, and issue recovery commands to such system.

19. (amended May 15, 2006) The apparatus of claim 13, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one hardware subsystem for generating a response of the system to failure; and wherein:

the circuits comprise portions for reacting to such response of such hardware subsystem.

20. (original) The apparatus of claim 13, particularly for use with a computing system that has plural generally parallel computing channels; and wherein:

the circuits comprise portions for comparing computational results from such parallel channels.

21. (amended May 15, 2006) The apparatus of claim 16, wherein:

the computing system has such parallel channels that are of diverse design.

[FOR THE BOARD'S CONVENIENCE: PLEASE SEE CLAIM 70, ADDED MAY 15, 2006 AND PREFERABLY FOR INSERTION HERE.]

22. (amended May 15, 2006) The apparatus of claim 13, particularly for use with a computing system that has plural processors; and wherein:

the circuits comprise portions for identifying such failure of any of such processors, based on error messages from such system, and for correcting for identified such failure.

23. (amended October 12, 2005) The apparatus of claim 13, wherein:

the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and handle a recovery command.

24. (amended October 12, 2005) The apparatus of claim 13, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; and wherein:

the circuits comprise portions for interposing analysis and a corrective reaction between such response-generating subsystem and such command-receiving subsystem.

25. - 32. (canceled)

33. (amended October 12, 2005) Apparatus for deterring failure of a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one hardware subsystem for generating an error message of the system about incipient failure; said apparatus comprising:

a network of components having terminals for connection to such system; and

circuits of the network for operating programs to guard such system from failure;

the circuits comprising portions for reacting to such error message of such hardware subsystem.

34. (amended October 27, 2005) The apparatus of claim 33, wherein:

in response to such error message, the circuits guard the entire such system from failure.

35. (amended October 12, 2005) The apparatus of claim 33, wherein:

the network is generic in that it can accommodate any such system that can issue an error message and handle a recovery command.

36. (original) The apparatus of claim 33, further comprising:

such computing system, including such hardware subsystem.

37. (amended May 15, 2006) The apparatus of claim 36, wherein:

the computing system has plural generally parallel computing channels; and

such parallel channels of the computing system are of diverse design or origin.

38. (amended May 15, 2006) The apparatus of claim 33, wherein:

said circuits are not capable of operating any application program; and are not controlled by any associated host computer that is capable of running any application program.

39. and 40. (canceled)

41. (amended October 12, 2005) The apparatus of claim 33, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; and wherein:

the circuits comprise portions for interposing analysis and a corrective reaction between such response-generating subsystem and such command-receiving subsystem.

42. (amended May 15, 2006) Apparatus for deterring failure of an entire computing system that is distinct from the apparatus and that has plural generally parallel computing channels and has at least one application-data input module, and at least one processor for running an application program; said apparatus comprising:

a network of components having terminals for connection to such system; and

circuits of the network for operating programs to guard such entire system from such failure, wherein the network is constructed to be initially and permanently distinct from such computing system including substantially (a) every such application-data input module and (b) every such application-program processor, and (c) all of such parallel computing channels;

the circuits comprising portions for comparing computational results from such parallel channels.

43. (original) The apparatus of claim 47, wherein:

the parallel channels of the computing system are of diverse design or origin.

44. (original) The apparatus of claim 42, wherein:

the comparing portions comprise at least one section for analyzing discrepancies between the results from such parallel channels.

45. (amended October 12, 2005) The apparatus of claim 44, wherein:

the circuits are not capable of running any application program.

46. (amended October 12, 2005) The apparatus of claim 42, wherein:

the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and computational results, and handle a recovery command.

47. (original) The apparatus of claim 42, further comprising:

such computing system.

48. (amended May 15, 2006) The apparatus of claim 42, wherein:

the circuits do not and cannot operate any application program; and are not controlled by any associated host computer that is capable of running any application program.

49. (amended May 15, 2006) The apparatus of claim 48, wherein:

to guard such entire system from failure, the circuits receive from such computing system error messages warning of incipient such failure and issue recovery commands to such computing system.

50. (amended May 15, 2006) Apparatus for deterring failure of an entire computing system that is distinct from the apparatus and that has plural generally parallel computing channels; said apparatus comprising:

a network of components having terminals for connection to such system; and

circuits of the network for operating programs to guard such entire system from such failure, wherein such network is constructed to be initially and permanently distinct from such computing system including all of such parallel computing channels;

the circuits comprising portions for comparing computational results from such parallel channels; and wherein:

the comparing portions comprise circuitry for performing an algorithm to validate a match that is inexact; and

the algorithm-performing circuitry employs a degree of inexactness suited to a type of computation under comparison.

51. (amended October 27, 2005) The apparatus of claim 50, wherein:

the algorithm-performing circuitry performs an algorithm that selects a degree of inexactness based on type of computation under comparison; and

the circuits also impose corrective action upon such system based upon discrepancies found by the comparing portions.

[CLAIMS 71 THROUGH 74 WERE ADDED MAY 15, 2006, PREFERABLY FOR INSERTION HERE.]

52. (amended May 15, 2006) The apparatus of claim 42, particularly for use with a computing system that has plural processors; and wherein:

the circuits comprise portions for identifying such failure of any of such processors and correcting for identified such failure.

53. (original) The apparatus of claim 42, wherein:

the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising:

at least three data-collecting and -responding modules, and

processing sections for conferring among the modules to determine whether any of the modules has failed.

54. (amended October 12, 2005) The apparatus of claim 42, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; and wherein:

the circuits comprise portions for interposing analysis and a corrective reaction between such response-generating subsystem and such command-receiving subsystem.

55. (amended May 15, 2006) Apparatus for deterring failure of any computing system that has plural processors and has at least one application-data input module, and at least one processor for running an application program, and is capable of generating an error message warning of incipient failure and capable of responding to a recovery command; said apparatus comprising:

a network of components having terminals for connection to such system, wherein the network is constructed to be initially and permanently distinct from such any computing system including substantially (a) every such application-data input module and (b) every such application-program processor, and (c) all of such plural processors; and

circuits of the network for operating programs to guard any such system from such failure;

the circuits comprising portions for identifying such failure of any of such processors and correcting for identified such failure.

[CLAIM 75 WAS ADDED MAY 15, 2006,
PREFERABLY FOR INSERTION HERE.]

56. (amended May 15, 2006) The apparatus of claim 75, wherein:

the identifying portions comprise a section that corrects for the identified such failure by taking a failed processor out of operation.

57. (amended October 12, 2005) The apparatus of claim 75, wherein:

the circuits cannot and do not run an application program.

58. (amended October 12, 2005) The apparatus of claim 75, wherein:

the circuits protect the entire such computing system.

59. (amended October 12, 2005) The apparatus of claim 75, further comprising:

such computing system.

60. (canceled)

61. (amended October 12, 2005) The apparatus of claim 75, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; and wherein:

the circuits comprise portions for interposing analysis and a corrective reaction between such response-generating subsystem and such command-receiving subsystem.

62. (amended May 15, 2006) Apparatus for deterring failure of an entire computing system that is distinct from the apparatus and has at least one application-data input module, and at least one processor for running an application program; said apparatus comprising:

a network of components having terminals for connection to such system; and

circuits of the network for operating programs to guard such entire system from such failure;

the circuits comprising modules for collecting and responding to data received from at least one of the terminals, said modules comprising:

at least three data-collecting and -responding modules, and

processing sections for conferring among the modules to determine whether any of the modules has failed;

wherein the network, including all of the modules and substantially (a) every such application-data input module and (b) every such application-program processor, and (c) all of the processing sections, is constructed to be initially and permanently distinct from such computing system.

63. (original) The apparatus of claim 62, further comprising:

such computing system.

64. (amended October 12, 2005) The apparatus of claim 62, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; and wherein:

the circuits comprise portions for interposing analysis and a corrective reaction between such response-generating subsystem and such command-receiving subsystem.

[CLAIMS 76 THROUGH 78 WERE ADDED MAY 15, 2006, PREFERABLY FOR INSERTION HERE.]

65. (amended May 15, 2006) Apparatus for deterring failure of a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; said apparatus comprising:

a network of components having terminals for connection to such system between the response-generating subsystem and the recovery-command-receiving subsystem; and

circuits of the network for operating programs to guard such system from such failure;

the circuits comprising portions for interposing analysis and a corrective reaction between the response-generating subsystem and the command-receiving subsystem.

66. (amended August 9, 2004) The apparatus of claim 65, further comprising:

such computing system.

67. (added October 12, 2005) The apparatus of claim 65, wherein:

the circuits cannot and do not run any application program.

68. (amended May 15, 2006) The apparatus of claim 65, wherein:

by responding to an error signal from such system, the circuits protect the entire such system from failure.

69. (added October 12, 2005) The apparatus of claim 65, wherein:

the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and handle a recovery command.

70. (amended May 15, 2006) The apparatus of claim 13, wherein:

the circuits do not and cannot operate any application program; and are not controlled by any associated host computer that is capable of running any application program.

71. (added October 12, 2005) The apparatus of claim 50, wherein:

the circuits cannot and do not run any application program.

72. (canceled)

73. (amended May 15, 2006) The apparatus of claim 50, wherein:

to guard such entire system from failure, the circuits receive from such computing system error messages warning of incipient failure and issue recovery commands to such computing system.

74. (added October 12, 2005) The apparatus of claim 50, wherein:

the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and computational results, and can handle a recovery command.

75. (added October 12, 2005) The apparatus of claim 55, wherein:

the program-operating circuits guard any such system from failure by issuing a recovery command; and

the failure-identifying and correcting portions provide the recovery command.

76. (added October 12, 2005) The apparatus of claim 62, wherein:

the circuits cannot and do not run any application program.

77. (amended May 15, 2006) The apparatus of claim 62, wherein:

to guard the entire such system from failure, the circuits receive from such computing system error messages warning of incipient failure.

78. (added October 12, 2005) The apparatus of claim 62, wherein:

the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and handle a recovery command.

79. (added October 27, 2005) The apparatus of claim 1, wherein:

the apparatus is not a circuit breaker.

80. (amended May 15, 2006) The apparatus of claim 1, wherein:

at least one of the network terminals is connected to receive at least one error signal generated by such system in event of incipient such failure of such system;

at least one of the network terminals is connected to provide at least one recovery signal to such system upon receipt of the error signal.

81. (amended May 15, 2006) An infrastructure for a computing system that has at least one computing node ("C-node") for running at least one application program; said infrastructure being for guarding the system against failure, and comprising:

at least one monitoring node ("M-node") for monitoring the condition of the at least one C-node by waiting for an error signal, indicating incipient such failure, from the at least one C-node and responding to the error signal by sending a recovery command to the at least one C-node; and

at least one adapter node ("A-node") for transmitting the error signal and recovery command between the at least one C-node and at least one M-node; and wherein:

the at least one M-node is manufactured, and remains, wholly distinct from the at least one C-node; and

the at least one M-node cannot, and does not, run any application program.

82. (added October 27, 2005) The infrastructure of claim 81, further comprising:

such computing system.

83. (added October 27, 2005) The infrastructure of claim 81, particularly for use with such computing system that has plural such C-nodes; and further comprising:

a decision-making node ("D-node") for comparing output data generated by such plural C-nodes and reporting to the at least one M-node any discrepancy between the output data; and wherein:

the at least one M-node analyzes the D-node reporting, and based thereon arbitrates among the C-nodes.

84. (allowed August 24, 2006) An infrastructure for a computing system that has at least one computing node ("C-node") for running at least one application program; said infrastructure being for guarding the system against failure, and comprising:

at least one monitoring node ("M-node") for monitoring the condition of the at least one C-node by waiting for an error signal, indicating incipient such failure, from the at least one C-node and responding to the error signal by sending a recovery command to the at least one C-node;

at least one adapter node ("A-node") for transmitting the error signal and recovery command between the at least one C-node and at least one M-node; and wherein:

the at least one M-node is manufactured, and remains, wholly distinct from the at least one C-node, and

the at least one M-node cannot, and does not, run any application program; and

at least one self-checking node for startup, shutdown and survival ("S3-node"), specifically for executing power-on and power-off sequences for such system and for the infrastructure, and for receiving error signals and sending recovery commands to the at least one M-node.

(11) EVIDENCE APPENDIX Page

Appellant has filed two pieces of evidence — each (by coincidence) being seventeen pages long:

- The expert Declaration of Jean-Claude Laprie, Doctor es-Science — filed June 5, 2006 and acknowledged by Examiner Bonzo in his Official Action dated August 24, 2006. As required, a copy of that Declaration appears as the immediately following 17 pages (Appeal Brief pages 76 through 92).

- A listing of 408 issued U. S. patents all of which contain, in the claims. the phrase "substantially exclusively" — filed in this case November 22, 2006 and shown in the PAIR website. As required, a copy of that listing appears as 17 pages following the Laprie Declaration (Appeal Brief pages 93 through 109).

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Algirdas Avizienis	Group Art Unit:	
Serial No.:	09/886,959		
Filed:	June 20, 2001		2613
Title:	"SELF-TESTING AND -REPAIRING FAULT-TOLERANCE INFRASTRUCTURE FOR COMPUTER SYSTEMS"		
Our docket:	xAAA-02	Examiner	Bryce P. Bonzo

DECLARATION OF JEAN-CLAUDE LAPRIE, Doctor es-Science

Hon. Asst. Commissioner for Patents
P. O. Box 1450
Arlington VA 22313-1450

Sir:

I, Jean-Claude Laprie, declare as follows.

1. I am a Directeur de Recherche (Director of Research) at the French National Organization for Scientific Research ("CNRS") in Toulouse — and particularly its Laboratory for System Analysis and Architectures ("LAAS").

2. I am a specialist in computer reliability, dependability, fault tolerance, and security.

3. I joined LAAS-CNRS in 1968. Here I founded the research group on fault tolerance and dependable computing in 1975, and directed that group until I became the director of LAAS in 1997.

4. My research has focused on dependable computing since 1973, and especially on fault tolerance and on dependability evaluation — subjects on which I have authored and coauthored more than a hundred papers, while also coauthoring or editing several books.

5. I have no monetary interest in the present patent application, and no financial interest in the affairs of the Applicant, Dr. Avizienis — and no other reason for favorable bias toward him that would prejudice my statements in this declaration. In years past, I coauthored some papers with him; this past collaboration in no way clouds my objectivity toward this subject matter in general, or his inventions specifically. My participation in this proceeding by declaration is without compensation, as part of the general exchange of personnel evaluations, literature critique etc. — among academic colleagues — again without any implication of bias.

6. I have been very active in the formulation of the basic concepts of dependability and the associated terminology; the views developed being widely adopted by the scientific community. My activities have included many collaborations with industry, culminating in the 1992 foundation of the Laboratory for Dependability Engineering ("LIS"), a joint academia-industry laboratory, that I directed until 1996.

7. I have also been very active in the international community, including the chairmanship of the IEEE Computer Society Technical Committee on Fault-Tolerant Computing in 1984-1985, of the International Federation for Information Processing ("IFIP") Work Group 10.4 on Dependable Computing and Fault Tolerance from 1986 to 1995, and of IFIP Technical Conference 10 on Computer System Technology from 1997 to 2001.

8. I am currently a vice-president of IFIP, and the representative of France in the IFIP General Assembly.

9. My honors include receipt of the IFIP "Silver Core" in 1992, the Silver Medal of the French Scientific Research in 1993, and the National Merit Medal in December 2002.

10. In summary, I am an internationally recognized expert and authority in the field of computing reliability.

11. In 2000 in New York City, at the Dependable Systems and Networks Conference, when Dr. Avizienis presented his technical paper on the system and methods that are the subject of this patent application, I was impressed with its innovativeness and its distinctive inventiveness — and I was one of several experts in this field who told him so.

12. As I understand it, Dr. Avizienis's patent application contains dozens of claims, and all but one are rejected. I am told that the grounds of rejection differ, for the many different claims, but do have several <u>common points</u> that are repeated.

13. In order to contribute to the dialogue, I have studied just a few claims that I am told are representative of all the claims, and whose rejections I am told are representative of all the rejections. I have also studied those rejections.

14. Based upon my expertise in this field as described above, I shall comment on the rejections of those representative claims. The representative claims are: claims 3, 18, 33, and 46.

15. I understand that one of these claims is "independent" *i. e.*, stands alone without referring to other claims. That is claim 33.

16. I also understand that the others of these claims are "dependent" — they cannot stand alone, but necessarily incorporate by reference some features that are recited in related independent claims. Therefore in discussing the dependent claims (claims 3, 18 and 46) I shall also comment on their associated independent claims (those are claims 1, 13 and 42).

17. CLAIM 3 — This claim, with its related independent claim 1, reads thus:

1. Apparatus for deterring failure of a computing system; said apparatus comprising:
a hardware network of components, having substantially no software and substantially no firmware except programs held in an unalterable read-only memory;
terminals of the network for connection to such system; and
fabrication-preprogrammed hardware circuits of the network for guarding such system from such failure.

3. The apparatus of claim 1, wherein:
the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and handle a recovery command.

18. On one hand, I understand that the phrase "computing system" refers to the computer(s) to be protected against failure. On the other hand, I understand that the terms "apparatus", "hardware network of components", "terminals" and "circuits" all refer to Dr. Avizienis's infrastructure invention, or parts of it.

19. I understand that the patent Examiner has cited against the representative claims (a) a patent issued to a man named Best, in combination with (b) Dr. Avizienis's own 1985 paper which discusses the Design Diversity Experiment ("DEDIX"). I have read and carefully considered the portions of both those documents on which the Examiner's rejections rely.

20. I see that the Examiner's discussion (in his "Official Action") of claim 3 says:

> **Best does not disclose, while Avizienis [1985] teaches:**
> **at least one of the network terminals is connected to receive one error signal generated by such system in event of incipient failure of such a system (page 1498 describes how the Decision and Executive layer receives exceptions from the version layer indicating errors within the instance running that particular version of the software);**
> **at least one of the network terminals is connected to provide one recovery signal to such system upon receipt of the error signal (page 1498 describe[s] the use of the local executive processing faults and providing [a] solution to the problem); and**
> **the apparatus further comprises means for automatically responding to the at least one error signal by generating the at least one recovery signal for guarding all such system against failure (page 1498 discloses the local and global executives at differing levels providing commands to the version which prevent[s] failure).**

21. That passage specifically addresses claim 3, but the Examiner's discussion continues with the following paragraph. (I understand that the entire paragraph below is thereafter also replicated verbatim with regard to some twenty other rejections.)

> **Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29); column 4, lines 14-25). Best further discloses that his system is [*sic*, has?] application to all types of digital systems (column 6, lines 29-61) and further are [*sic*] . . . applicable at any level (column 6, lines 42-47). Avizienis teaches the use of the DEDIX**

QCL

distributed data processing system, and more importantly that is [*sic*, it?] may implemented [*sic*] in single computer and multiple computer [*sic*] acting in concert across a network (page 1497, column 2). Avizienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avizienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avizienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend [*sic*, intent?] to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avizienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor [*sic*] it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the fault tolerant portions of the layered DEDIX system of Avizienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-version software system.

22. Thus the Examiner appears to propose that a person skilled in the computer field would find the apparatus of Dr. Avizienis's claim 3 "obvious" as a combination of certain features of Best with certain features of Dr. Avizienis's own 1985 paper.

23. After pondering the Examiner's two passages above, and carefully studying the cited parts of those two earlier documents, I sincerely cannot agree. Here is why:

24. First, <u>neither</u> of the two reference documents even satisfies the recitation of the underlying independent claim 1: "a hardware network of components, having substantially no software . . . ." Best makes absolutely clear that his product is "under software control" and has a host processor (though it is vaguely defined, it evidently runs software); and DEDIX is <u>entirely</u> software.

25. Therefore, as a completely independent expert in this field, with apologies I find it difficult to understand how there can be any argument about this extremely simple technical point.

JCL

26. Second, the Examiner's notes reveal several misunderstandings of the character of the systems in the two references, vis-a-vis the claim-3 language (emphasis added): "the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and handle a recovery command." This is a very simple and short clause, but the Examiner talks all around it (see paragraphs 20 and 21 above) without ever confronting it directly.

27. As I read the Avizienis 1985 discussion of the DEDIX, that experiment was set up to deal with a very specific class of software modules that were custom-designed for the experiment. They were specially fitted with very unusual cross-check features, to enable the *N*-version software comparisons in the experiment. Similarly, many other kinds of software modules would not be compatible with the DEDIX at all.

28. The cross-check provisions of the DEDIX required that each participating program of the *N* versions contained specifically formatted "cross-check vectors" ("cc-vectors") that the DEDIX could recognize. Furthermore they had to be at particular points in the program, where data were comparable as between versions. A program lacking these cc-vectors — at the right locations — could not run properly in the DEDIX. Thus it is quite wrong to call the DEDIX "generic in that it can accommodate any such system that can issue an error message and handle a recovery command." Note too that a cc-vector was not an "error message".

29. Best likewise is controlling a set of circuit modules that are extremely distinctive, and the control signals from

their associated software are custom-designed to operate those particular circuit modules. Thus neither of the two cited references answers to the simple, direct language of claim 3.

30. Paragraphs 24 through 29 above give two reasons to question the purported "obviousness" of claim 3 in view of the Avizienis/Best combination: neither reference meets the underlying claim-1 limitations, and neither reference meets the plain claim-3 limitations. Although I believe that each one of these reasons alone is fatal to the Examiner's argument, I will discuss below (in paragraphs 31 through 40) yet a third reason that is more directly responsive to the Examiner's sophisticated arguments: the documents do not inspire a person who knows this field to make the combination.

31. Third, as I have indicated just above, a person who is skilled in this field and looks at the two documents will not likely be moved to combine any of their features.

32. One document describes a trivial hardware circuit for manufacture, practical application and ongoing use. The other describes a distributed operating system — closely supervised by many scientists working in parallel — for a one-time academic experiment about executing and debugging multiple-version software systems.

33. I do understand, and I will grant, that under some circumstances a patent examiner normally may be at liberty to disregard such practicalities and basics. In this situation, however, the issue seems to be what a real person skilled in

JCL

the field would perceive or realize about possible "combinations" — and to that issue, I can testify with confidence.

34. In truth, in the real world, such a person's thinking is illuminated by the relationships that suggest themselves from reading the two documents. In this case, virtually no relevant relationships suggest themselves. The concepts, and especially the documents, are just too disparate.

35. In fact, even upon being told that it is suggested to somehow combine the two, someone skilled in this field must immediately wonder why.

36. The purported linkage is just not real, and in fact it is almost incomprehensible to me how the DEDIX experiment could be implemented in hardware, or Best could be expanded into an *N*-version software experiment, or why.

37. In an early section of Dr. Avizienis's 1985 paper — not discussing the DEDIX — he does suggest that a general-purpose computer could be improved by including two additional instructions in the instruction set: "take majority vote", and "cross-check" data (at the cross-check points). Such proposed instructions might be regarded as "hardware support" for software voting, but the Examiner's argument that Avizienis suggested "hardware voting" is flatly incorrect. The Avizienis '85 paper suggests neither (a) hardware voting nor (b) combination of an *N*-version software experiment with hardware voting.

38. Still as to the third reason for believing that it would not be obvious to combine Best with Avizienis '85: although it

would not occur to a person in this field to combine them, ironically the insertion of Best into the DEDIX also would be superfluous. The DEDIX already has voting functions.

39. I see no reason to believe that Best's voting hardware, with associated software modules to run it, would be any better than the all-software voting provisions already present in the DEDIX. Therefore even if it did, for some incomprehensible reason, occur to a skilled computer engineer to combine the two ideas, that person would immediately reject the idea.

40. Furthermore as a practical matter the importation of Best's hardware, or its conceptual equivalent, into the multiple-minicomputer network running DEDIX would pose major practical problems. Not only would an instance of Best's hardware have to be electronically linked with each one of the minicomputers, but in addition Best's control software would have to be somehow integrated into the existing DEDIX software — and all to no particular avail, since the hardware implementation (as I have stated above) offers no benefit.

41. CLAIM 18 — This claim, with its independent claim 13, reads as follows. (Please note the ellipsis ". . ." at line *c* — where several lines have been omitted because they are not related to the Best patent or the Avizienis 1985 paper.)

a 13. Apparatus for deterring failure of an entire computing system, wherein the computing system
b optionally includes plural mutually redundant modules; said apparatus comprising:
c a network of components having terminals for connection to such system, . . . ; and
d circuits of the network for operating programs to guard such entire system from such failure;
e the circuits comprising portions for identifying such failure of any of the circuits and
f correcting for the identified such failure.

a 18. The apparatus of claim 13, wherein:
b said circuits receive from such system error messages warning of incipient such failure, and
c issue recovery commands to such system.

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42. The assertion by the Examiner as to claim 18 is:

> **Best does not disclose, while Avizienis teaches:**
> **said circuits receive from such system error messages warning of incipient failure, and issue recovery commands to such system (page 1498 discloses specific application and OS error recovery commands handled by the Local executive, while Best discloses substituting the correct data onto the channel).**

This comment is followed by yet another copy of the longer paragraph quoted previously.

43. First, in my professional opinion neither Best nor the 1985 Avizienis paper answers to the language of the independent claim, claim 13. In support of this statement, I note:

44. Best does not deter or guard against failure of an "entire" computing system, and indeed never even discloses the basic character of the computing system — it is at most only implicitly present.

45. Since Best presents almost no information about the computing system to be protected, certainly he does not suggest that his modest invention can protect that (or any other) "entire" computing system. His invention relates to only those small parts (the "communication channels") of a computer network that pass messages, nothing more.

46. As to Dr. Avizienis's discussion of the DEDIX experiment, it was not the particular purpose of that academic experiment to guard against failure — but rather to monitor and study failure.

47. For the purposes of academicians, the experiment evidently was run unattended for relatively brief periods (e. g. overnight or on a weekend), and would collect errors for study

and analysis. It would also allow the supervising experimenters to debug the many ("*N*") program versions involved, individually.

48. Thus any possible effect which the experiment may have had in "deterring failure" of its individual program versions was incidental to its primary functioning — namely to learn what could be learned about the parallel operation of multiple program versions. In other words in the DEDIX the deterrence of individual-version failure is a rather semantic question, revolving around the relative importance of primary purpose vs. the relative importance of incidental effects.

49. For present purposes, however, all of this is a moot point — because the language of claims 13 and 18 specifies "deterring failure of an <u>entire</u> computing system", and this the DEDIX certainly did not do. In no way could the all-software DEDIX prevent the entire system, consisting of some twenty minicomputers, from failing.

50. Since the specifics of claim 13 are understood to carry over to claim 18 as well, then claim 18 is likewise unable to read on Best, or DEDIX, or any combination of the two. (Once again I find the idea of combining these two documents very <u>un</u>obvious to a person skilled in the computer field.)

51. CLAIM 33 — This claim is independent:

33. Apparatus for deterring failure of a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one hardware subsystem for generating an error message of the system about incipient failure; said apparatus comprising:
a network of components having terminals for connection to such system; and
circuits of the network for operating programs to guard such system from failure;
the circuits comprising portions for reacting to such error message of such hardware subsystem.

52. As to this claim, the Examiner again asserts (questionably) that Best's apparatus deters failure "of a computing system", and includes circuits "for operating programs to guard such system from failure". The Examiner then comments further:

> Best does not disclose, while Avizienis teaches:
> Apparatus [*sic*, "a computing system"] that is substantially exclusively made of commercial, off-the-shelf components and that has at least one hardware subsystem for generating an error message of the system about incipient failure (page 1498 describes the Version layer reporting errors and receiving decisions results),
> the portions for reacting to such error messages of such hardware system (1498 discloses the Local and global executives performing these functions).

53. I disregard the apparent typographical error, in which the Examiner at first seems to mistakenly attribute the all-COTS construction and the hardware subsystem to the "apparatus" rather than the claimed "computing system". I think it is clear what he meant.

54. Here too, however, it appears to me that the analysis is badly off target. The truth is that the version layer of the DEDIX, as described by Avizienis, does not have "at least one hardware subsystem for generating an error message . . . about incipient failure". My statement here is correct for the "version layer" in Fig. 2 of Avizienis as well as the general "version J" in Fig. 1.

55. The DEDIX is an all-software experimental arrangement — using essentially standard minicomputers operated by its aca-

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demic participants. All of the *N* versions in the "version layer" of the DEDIX are likewise all software. There is no ASIC for generating error messages. Therefore it does not make sense to me to describe any part of these general-purpose minicomputers, or any part of the software running in them, as "a hardware subsystem".

56. In my professional opinion it is improper to strain the normal definitions of computer-system elements in this way, in an effort to "prove" that a person of ordinary skill in the field would find it obvious to combine teachings of two references. The definition implied here is overbroad and therefore unfair.

57. I think such argumentation departs unreasonably from a patent Examiner's prerogative to adopt a broad but fair reading of claim language. In real life, a person skilled in the computer field would not recognize, or acquiesce in, such strained definitions of ordinary elements.

58. CLAIM 46 — This claim, with its independent claim 42, reads thus (here too, at the ellipsis ". . ." in line *g*, several irrelevant lines have been omitted):

a 42. Apparatus for deterring failure of an entire computing system that is distinct from the
b apparatus and that has plural generally parallel computing channels and has at least one
c application-data input module, and at least one processor for running an application program; said
d apparatus comprising:
e a network of components having terminals for connection to such system; and
f circuits of the network for operating programs to guard such entire system from such failure,
g . . . ;
h the circuits comprising portions for comparing computational results from such parallel
i channels.

a 46. The apparatus of claim 42, wherein:
b the network is an infrastructure which is generic in that it can accommodate any such system
c that can issue an error message and computational results, and handle a recovery command.

JCL

59. I have commented above on the "entire computing system" concept. That previous comment applies also to claim 42.

60. The patent Examiner makes short work of claim 46, but to me his statements about this claim are simply wrong. He says:

> **Best does not explicitly disclose, while Avizienis teaches:**
> **the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and handle recovery command (page 1498; DEDIX hides all the fault processing from the version layer, and it is the decision and executive layer which performs this functionality, making it generic).**

61. First regarding the language of independent claim 42, as I have pointed out above, the DEDIX did not and could not deter failure of an "entire" system. (At the very most it could incidentally deter failure of some subcomponents of its multiple versions, and not as its major purpose — and even then only for short time intervals between supervisory interventions by its experiment operators.)

62. Second, regarding the language of dependent claim 46, as I have pointed out above, neither Best nor the DEDIX could accommodate "any" system that could issue an error message and handle a recovery command; rather, both of these reference inventions were able to service only very narrowly defined and prepared (basically "custom") systems.

63. Actually I think the DEDIX network was not truly an infrastructure at all. In my view an infrastructure provides to a computing system all the necessities for operation, including power, active isolation from potentially hostile physical environments, and (particularly in the case of the present invention) fault tolerance — *i. e.*, ability to continue functioning in the presence of faults, including for instance hacker attacks. The DEDIX was not an infrastruc-

ture but rather in the nature of an intermediate-level operating system (or operating subsystem), being built upon a basic layer of Unix as shown in the diagrams.

64. Third, the Examiner's brief statement about claim 46 seems to go through the motions of a logical process; but, as I see it upon careful reflection, the conclusions do not follow from the premises — and, what is more, are not correct.

65. To be specific, the fact that fault processing is hidden from the version layer proves virtually nothing. In particular it does not imply that the DEDIX network can accommodate any system (or any system which can issue error messages and handle recovery commands).

66. Similarly the fact that the decision and executive layer performed the hiding or provided error messages does not prove that the DEDIX was "generic" in the sense defined in claim 46.

67. Therefore it strikes me as reckless, and also definitely not correct, to state with authority that the DEDIX "is an infrastructure which is generic in that it can accommodate any such system".

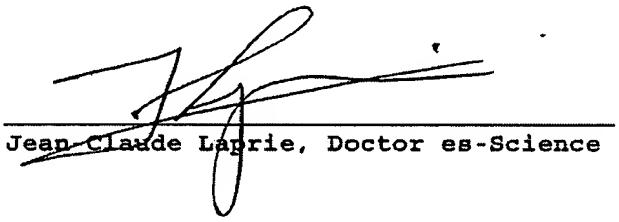
68. After his brief paragraph, quoted just above, about claim 46, the Examiner again replicates his long paragraph about combining teachings of the two references. For reasons stated earlier, I object to this combining. I find the idea of constructing such a combination bizarre.

JCL

69. My remarks about "all hardware" construction, and about protecting an all-COTS computing system, and about generically protecting "any system", and about receiving an error message and returning a recovery command, and about protecting an "entire system" of course apply to other claims that recite substantially the same features, respectively.

All statements herein made of my own knowledge are true; all statements made on information and belief I believe to be true. I understand that willful false statements and the like herein are punishable by fine or imprisonment, or both (18 U.S.C. 1001) and may jeopardize the validity of the subject application or any patent issued thereon.

May 29, 2006
date



Jean-Claude Laprie, Doctor es-Science

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	PAT. NO.	Title
1	7,134,737	Closed-loop color correction using factory-measured color cutoffs anchored to field-measured white point
2	7,105,148	Methods for producing hydrogen from a fuel
3	7,096,673	Blade tip clearance control
4	7,081,135	Mastopexy stabilization apparatus and method
5	7,066,734	Convertible dental instrument
6	7,052,338	Integral reversing and trim deflector and control mechanism
7	7,017,426	Coupler arrangement for isolation arrangement for system under test
8	6,998,774	Electrically insulated electroluminescent display
9	6,990,175	X-ray computed tomography apparatus
10	6,979,508	Fuel cell with integrated feedback control
11	6,972,156	Body formed of set, initially pasty material and including an electrically conducting path and a method of making such a body
12	6,951,578	Polycrystalline diamond materials formed from coarse-sized diamond grains
13	6,951,553	Tissue closure treatment system and method with externally-applied patient interface
14	6,936,037	Tissue closure treatment system, patient interface and method
15	6,924,701	Method and apparatus for compensating an amplifier
16	6,877,932	Drainage system and method for artificial grass using spacing grid
17	6,874,193	Inhibitor dispensing pipeline pig
18	6,872,308	Condensate polisher with deep cation bed and powdered resin bed
19	6,856,390	Time-delay integration in electrophoretic detection systems

[Appeal-Brief page 93]

20 6,832,025 Fiber bragg grating fabrication method
21 6,823,946 Horse-shoe type, plate-shaped, plastic hoof fitting
22 6,821,456 Granular polymer additives and their preparation
23 6,809,007 Method and a carrier for treating end facets in photonic devices
24 6,794,647 Mass analyzer having improved mass filter and ion detection arrangement
25 6,782,640 Custom conformable device
26 6,777,098 Marking of an anodized layer of an aluminium object
27 6,762,683 Tag device
28 6,756,290 Method for the production of a semiconductor device
29 6,755,022 Turbo-charged internal combustion engine with in-cylinder EGR and injection rate shaping
30 6,746,752 Synthetic grass with resilient granular top surface layer
31 6,717,813 Heat dissipation unit with direct contact heat pipe
32 6,712,830 Soft tissue anchor
33 6,688,587 Method for the adaptation of a machine support
34 6,679,882 Electrosurgical device for coagulating and for making incisions, a method of severing blood vessels and a method of coagulating and for making incisions in or severing tissue
35 6,666,225 System and method for optimizing the efficiency of an oil supply
36 6,653,148 Optical sensor for determining an analyte, and method of manufacturing the optical sensor
37 6,644,252 Two-stroke engine with storage duct
38 6,638,470 Flash-spinning process and solution
39 6,636,306 Optical spectrum analyzer
40 6,627,976 Leadframe for semiconductor package and mold for molding the same
41 6,625,945 Balanced, multi-stud hold-down
42 6,624,577 Tungsten-rhenium filament and method for producing same
43 6,590,183 Marking of an anodized layer of an aluminum object
44 6,586,443 Method of treating multiple sclerosis
45 6,576,084 Method of pretreating pulp with yield or strength-enhancing additive
46 6,551,689 Synthetic grass with resilient granular top surface layer
47 6,541,066 Thin ceramic coatings
48 6,527,916 Pressing section for a paper machine
49 6,517,684 Method of producing moulded pulp articles with a high content of dry matter
50 6,516,168 IMAGE FORMING APPARATUS, A CARTRIDGE AND DEVELOPER CONTAINER DETACHABLY MOUNTABLE THEREON, AND A DRIVING SOURCE FOR PROVIDING A FORCE FOR OPENING A SEALING MEMBER FOR REMOVABLY SEALING A DEVELOPER SUPPLYING OPENING

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	PAT. NO.	Title
51	6,515,052	Granular polymer additives and their preparation
52	6,498,862	Evaluation of biofilms and the effects of biocides thereon
53	6,496,093	Displacement device
54	6,488,892	Sample-holding devices and systems
55	6,469,311	Detection device for light transmitted from a sensed volume
56	6,460,264	Part Measurement test fixture
57	6,443,513	Cup bumper absorber
58	6,435,682	Laser imaging using a spatial light modulator
59	6,418,256	High order spatial mode optical fiber
60	6,387,074	Two-chamber drug delivery device comprising a separating membrane
61	6,367,473	Medium dispenser
62	6,367,049	Encoding multiword information by wordwise interleaving
63	6,352,331	Detection of non-firing printhead nozzles by optical scanning of a test pattern
64	6,338,682	Portable, adjustable-contour, putting green
65	6,336,330	Steam-turbine plant
66	6,332,221	Thermoregulatory clothing
67	6,328,286	Apparatus for blowing streams of bubbles
68	6,323,949	Optical measurement method and apparatus which determine a condition based on quasi-elastic-interaction
69	6,317,207	Frequency-domain light detection device

[Appeal-Brief page 95]

70 6,297,018 T Methods and apparatus for detecting nucleic acid polymorphisms
71 6,276,375 T Apparatus and methods for washing cores of cored lettuce heads
72 6,270,104 T Composite bicycle frame and methods for its construction
73 6,264,244 T End connector for composite coiled tubing
74 6,257,454 T Media dispenser
75 6,236,508 T Multicolor detector and focal plane array using diffractive lenses
76 6,219,087 T Interactive video communication in real time
77 6,187,267 T Chemiluminescence detection device
78 6,182,673 T Dump facility for cassette sewage tanks
79 6,182,515 T Coupler arrangement for isolation arrangement for system under test
80 6,179,141 T Container assembly provided with anitbacterial agent against slow-leak bacteria
81 6,178,008 T Constructing device-state tables for inkjet printing
82 6,153,442 T Reagents and methods for specific binding assays
83 6,132,556 T Method of controlling pulp digester pressure via liquor extraction
84 6,125,318 T Slip ratio antiskid controller using mu/slip ratio generated velocity reference
85 6,107,925 T Method for dynamically adjusting criteria for detecting fire through smoke concentration
86 6,086,181 T Maximum-diagonal print mask and multipass printing modes, for high quality and high throughput with liquid-base inks
87 6,086,151 T Chair apparatus with resilient support member
88 6,079,093 T Method and device for releasing cathode plates
89 6,078,922 T Market research database having historical control designator
90 6,071,748 T Light detection device
91 6,052,628 T Method and system for continuous motion digital probe routing
92 6,037,849 T Microwave switch having magnetically retained actuator plate
93 6,034,008 T Flash-spun sheet material
94 6,029,961 T Sleeve-type rubber shock absorber with hydraulic damping
95 6,026,992 T Media dispenser
96 5,992,703 T Dispenser for discharging media
97 5,991,055 T Underpulsed scanner with variable scan speed, P. W. M. color balance, scan modes and column reversal
98 5,989,712 T Process for treating a body of stainless steel so as to promote its adherence to a rubber composition
99 5,980,741 T Bubble trap with flat side having multipurpose supplemental ports
100 5,973,673 T Cursor control device

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	PAT. NO.	Title
101	5,969,591	Single-sided differential pressure sensor
102	5,958,527	Process of laying synthetic grass
103	5,958,161	Process for treating a body of stainless steel so as to promote its adherence to a rubber composition
104	5,948,376	Catalyst for purifying exhaust gases
105	5,943,219	System for providing air flow control and EMC shielding of front panels of computers and similar electronic equipment
106	5,941,418	Multiple fluid dispensing system
107	5,935,519	Apparatus for the detection of sulfur
108	5,934,698	Adjustable hitch support
109	5,933,977	Curl control with dryer aircaps
110	5,901,883	Dispenser having nozzle insert with passages for discharge of two media
111	5,884,819	Dispenser for media
112	5,884,775	System and method of inspecting peel-bearing potato pieces for defects
113	5,878,538	Device, particularly for compensating the internal and external pressures in a double-glazing unit
114	5,870,021	Annealing magnetic elements for stable mechanical properties
115	5,863,175	Loading device for material rolls, particularly for paper rolls
116	5,851,936	Elongation for flash spun products

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117 5,825,102 Fail-safe circuit
118 5,813,993 Alertness and drowsiness detection and tracking system
119 5,809,883 Drive for a plurality of transfer cylinders of a printing machine
120 5,799,620 Direct contact fluid heating device
121 5,791,518 Dispenser for discharging media
122 5,791,338 Endotracheal intubation apparatus
123 5,786,688 Electrical ammeter including an induction coil
124 5,779,706 Surgical system
125 5,768,482 Resolution-triggered sharpening for scaling of a digital-matrix image
126 5,767,770 Semi-hard magnetic elements formed by annealing and controlled oxidation of soft magnetic material
127 5,740,841 Can filling apparatus
128 5,727,933 Pump and flow sensor combination
129 5,723,055 Nozzle assembly having inert gas distributor
130 5,722,589 Composite load bearing structure
131 5,712,990 Economical automated process for averting physical dangers to people, wildlife or environment due to hazardous waste
132 5,708,740 Optical notch filter manufacture in optical fibre waveguide by plastic deformation
133 5,697,926 Cautery medical instrument
134 5,692,597 Conveyor belt assembly
135 5,677,405 Homopolymers and copolymers of cationically polymerizable monomers and method of their preparation
136 5,669,623 Baby carriage and method of manufacturing seat plate for its seat
137 5,667,566 Apparatus for water vapor removal from a compressed gas
138 5,662,996 Method for manufacturing self-supporting synthetic trim parts and thus manufactured trim parts
139 5,651,235 Packaging method and apparatus
140 5,637,386 Fining abrasive materials
141 5,628,563 Method and system for slurry preparation and distribution
142 5,625,502 Mirror pivoting mechanism, and vehicle comprising such mirror pivoting mechanism
143 5,615,456 Tolerance-compensating reusable clamp structure
144 5,609,295 Composite railway tie and method of manufacture thereof
145 5,601,539 Microbore catheter having kink-resistant metallic tubing
146 5,593,546 Hybrid former with an MB unit in a paper machine
147 5,592,833 Process and apparatus for the recovery of pure argon
148 5,588,017 Optoelectronic semiconductor device, system for optical glass fibre communication having such a device, semiconductor diode laser for use in such a device, and method of manufacturing such a device
149 5,579,933 Safety container and dispenser for small items
150 5,577,131 Device for segmenting textured images and image segmentation system comprising such a device

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151	5,574,068	S-nitrosothiols as smooth muscle relaxants and therapeutic uses thereof
152	5,570,444	Method of optically coupling optical fibres to injection lasers
153	5,561,134	Compounds having antihypertensive, cardioprotective, anti-ischemic and antilipolytic properties
154	5,554,096	Implantable electromagnetic hearing transducer
155	5,535,999	Apparatus for rotating a flat article through a desired angular orientation
156	5,531,283	Drivetrain and load bearing swivel hitch assemby and combine incorporating same
157	5,525,181	Method of manufacturing a multilayer printed circuit board having first and second conducting patterns connected through an adhesive layer and laminate for the manufacture of such a printed circuit board
158	5,524,700	Method of and vessel for filling a casting mold
159	5,520,337	Controllable discharge head for controlling the flow media delivered therethrough
160	5,513,033	Optical fibre amplifier
161	5,510,806	Portable computer having an LCD projection display system
162	5,506,452	Power semiconductor component with pressure contact
163	5,498,853	Heater, particularly for kitchen appliances
164	5,495,216	Apparatus for providing desired coupling in dual-mode dielectric resonator filters
165	5,485,767	Saw blade machining system
166	5,475,894	Handgrip for a tool and method of making same

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167 5,475,361 Strobe warning light
168 5,469,989 Dispenser for positively discharging a medium through a plurality of motions
169 5,464,319 Regenerative pump with an axially shifting working fluid chamber
170 5,459,298 Surgical system temperature controlled electric heating tool
171 5,456,654 Implantable magnetic hearing aid transducer
172 5,443,185 Dispenser for media
173 5,439,113 Bulk container
174 5,430,845 Peripheral device interface for dynamically selecting boot disk device driver
175 5,420,902 Fuel assembly with a flow-aiding spacer
176 5,402,952 Tube coupling system for a spinning or twisting spindle
177 5,402,799 Guidewire having flexible floppy tip
178 5,401,520 Apparatus and method for defrosting frozen proteinaceous food blocks
179 5,393,958 Heater with a pretensioned heating element
180 5,384,996 Architectural joint system with arched cover plate
181 5,383,568 Method and article for packaging paper and the like
182 5,375,745 Media dispenser with initial pressure-relief state
183 5,364,862 Compounds having antihypertensive and anti-ischemic properties
184 5,356,900 Method of treating chronic herpes virus infections using an opiate receptor antagonist
185 5,355,971 Drivetrain and load bearing swivel hitch assembly and combine incorporating same
186 5,355,935 Method and device for vibrating an ingot mould for the continuous casting of metals
187 5,345,951 Smoking article
188 5,336,111 Boardlock for an electrical connector
189 5,335,658 Intravascular blood parameter sensing system
190 5,333,728 Compact disc jacket and blank therefor
191 5,330,082 Threaded dispensing closure with flap
192 5,326,599 Cabin purge system for automotive powder coating
193 5,321,381 Base for an electromechanical functional unit
194 5,314,173 Fluid-filled elastic mount having vacuum-receiving chamber partially defined by elastic member for isolating high-frequency vibrations
195 5,310,526 Chemical sensor
196 5,300,129 Coating for improved retention of cbn in vitreous bond matrices
197 5,294,076 Airship and method for controlling its flight
198 5,289,946 Dispenser for media
199 5,269,582 Convertible top
200 5,267,687 Two way mailer

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	PAT. NO.	Title
201	5,260,773	Color alternating 3-dimensional TV system
202	5,254,061	Eddy current braking system
203	5,252,884	Translation device
204	5,251,761	Method of collecting recyclable materials
205	5,248,032	Compact disc jacket
206	5,246,212	Fluid-filled elastic mount having vacuum-receiving chamber and auxiliary air chamber for accommodating volumetric change of equilibrium chamber
207	5,241,012	Activated and conjugated polystyrene substrate
208	5,238,630	In-mold labeling method
209	5,228,586	Media dispenser with removable use index
210	5,226,599	Flush sprinkler
211	5,225,087	Recovery of EDTA from steam generator cleaning solutions
212	5,223,569	Self-adhesive conductive elastic gel
213	5,217,211	Fluid-filled elastic mount having vacuum-receiving chamber partially defined by flexible diaphragm with rigid restriction member
214	5,216,321	Shadow-mask type color cathode-ray tube
215	5,208,867	Voice transmission system and method for high ambient noise conditions
216	5,202,482	Malignancy-associated catabolite
217	5,191,133	Process for preparation of 2-vinylnaphthalene
218	5,184,449	Method of and apparatus for the wrapping of palletized units

[Appeal-Brief page 101]

219 5,181,483 T Automatically coupling fan for automative cooling systems
220 5,180,917 T Self-calibrating proportional counter
221 5,180,148 T Fluid-filled elastic mount having two orifices passages one of which is selectively opened and closed by means of vacuum pressure
222 5,174,283 T Blind orolaryngeal and oroesophageal guiding and aiming device
223 5,173,701 T Radar apparatus with jamming indicator and receiver device with jamming indicator
224 5,170,998 T Fluid-filled elastic mount having means for controlling elastic deformation of flexible diaphragm(s) defining equilibrium chamber(s)
225 5,167,403 T Fluid-filled elastic mount having two orifice passages one of which is selectively opened and closed by means of vacuum pressure
226 5,164,573 T Optical reading device
227 5,164,222 T CVD method for depositing a layer on an electrically conductive thin layer structure
228 5,158,272 T Work table having a metallic cutting base for an automatic fluid jet cutting installation
229 5,145,156 T Fluid-filled elastic mount having two differently tuned orifices selectively utilized for damping or isolating vibrations in different frequency ranges
230 5,141,278 T Window molding member for automobiles
231 5,137,155 T Method and an apparatus for treating plant fibres
232 RE33,970 T Cushioning device for remote control television equipment, and assembly thereof
233 5,122,639 T Electric hotplate
234 5,098,072 T Fluid-filled elastic mount having two differently tuned orifices and means for controlling pressure in air chamber or chambers adjacent to equilibrium chamber or chambers
235 5,087,010 T Speaker's prompting podium
236 5,082,311 T Passive impact restraining vehicular steering column assembly
237 5,078,607 T Dental implant including plural anchoring means
238 5,074,287 T Cervical traction device
239 5,072,741 T Method of and apparatus for simultaneously making plural tobacco filler streams
240 5,065,584 T Hot gas bypass defrosting system
241 RE33,729 T Multilayer optical filter for producing colored reflected light and neutral transmission
242 5,061,181 T Dental implant including plural anchoring means
243 5,052,622 T Sprinkler
244 5,046,197 T Molded plastic belt and buckle
245 5,038,766 T Blind orolaryngeal and oroesophageal guiding and aiming device
246 5,028,193 T Saddle-bound books, magazines and the like and process for manufacture same
247 5,015,900 T Motor support and method of making
248 5,013,739 T Method of treating chronic fatigue syndrome using an opiate receptor antagonist
249 5,006,946 T Flexible polymeric resinous magnetic head supporting device
250 5,001,583 T Flexible polymeric resinous magnetic head supporting device

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	PAT. NO.	Title
251	4,999,602	Resistor for audio/video signal circuit
252	4,997,235	Light metal wheel rim apparatus
253	4,993,526	Luggage-protective pad including integral feet and bumper
254	4,992,603	Process for producing nitromethane
255	4,959,674	Acoustic ink printhead having reflection coating for improved ink drop ejection control
256	4,953,989	Gas bearing part, and device provided with such a gas bearing part
257	4,937,638	Edge emitting light emissive diode
258	4,936,025	Combination infrared and airborne drying of a web
259	4,934,365	Non-invasive hyperthermia method and apparatus
260	4,921,516	Method of manufacturing optical fibers with elimination of paraxial refractive-index dip
261	4,917,971	Internal reforming fuel cell system requiring no recirculated cooling and providing a high fuel process gas utilization
262	4,904,164	Scroll type compressor with variable displacement mechanism
263	4,901,049	Temperature limiter
264	4,899,926	Two way mailer
265	4,888,346	Method for the treatment of persons infected with HTLV-III (AIDS) virus
266	4,872,738	Acousto-optic fiber-optic frequency shifter using periodic contact with a surface acoustic wave
267	4,863,073	Valve for aerosol container
268	4,858,579	Fuel-injection for direct-injection diesel engine

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269 4,854,776 T Process and apparatus for lining a tunnel with concrete
270 4,840,462 T Method of driving a ferroelectric liquid crystal display device and associated display device to achieve gray scale
271 4,839,032 T Separating constituents of a mixture of particles
272 4,832,825 T Method for the injection of catalyst in a fluid catalytic cracking process, especially for heavy feedstocks
273 4,821,497 T Cotton harvester and tandem row unit therefor
274 4,807,317 T Modular ramp
275 4,796,857 T Metallic seal for high performance butterfly valve
276 4,796,469 T Apparatus and process for measuring change of liquid level in storage tanks
277 RE32,722 T Ventilation system with thermal energy recovery
278 4,761,323 T Method and article for the production of porous fiber bats
279 4,742,689 T Constant temperature maintaining refrigeration system using proportional flow throttling valve and controlled bypass loop
280 4,715,335 T Internal combustion engine with reduced noise and heat emissions
281 4,708,230 T Declutching device
282 4,702,806 T Method of and apparatus for recovering a metal from a solution, namely an electrolyte-containing metal
283 4,701,639 T Threshold detector circuit and method
284 4,698,914 T Setting/drying process for flexible web coating
285 4,687,926 T Spectrally filtered lens producing plural f-numbers with different spectral characteristics
286 4,674,298 T Pendant necklace assembly including a disengageable writing implement
287 4,673,576 T Method of producing veal and animal feed therefor
288 4,669,022 T Magnetic-tape scanning device with improved rating transformer mounting and method of manufacturing such a device
289 4,662,372 T Disposable surgical instrument and method of forming
290 4,637,862 T Wire-glass composite and method of making same
291 4,634,852 T Sensor using fiber optic interferometer
292 4,633,344 T Unambiguously tracking a data track in response to signals derived from the track data itself
293 4,629,443 T Installation for damping torsional vibrations in a gear drive, especially between the crankshaft and an output shaft of internal combustion engines
294 4,627,654 T Articulated parallelogram gripper
295 4,626,191 T Method of controlling a combustion flame and a microphonic probe allowing the application of the method
296 4,619,404 T Gas distribution arrangement for the admission of a processing gas to an atomizing chamber
297 4,616,915 T Immersion type film processing apparatus
298 4,615,433 T Method of conveying particulate solids
299 4,601,211 T Multi-port valve in a gas collection system and method of using same
300 4,597,379 T Method of coagulating muscle tissue

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	PAT. NO.	Title
301	4,590,155	Emulsion having high silver chloride content, photographic recording material and process for the production of photographic recordings
302	4,581,913	Method for improving the release and finish characteristics of metal stamping dies
303	4,562,244	Process for forming thermally stable thermotropic liquid crystalline polyesters of predetermined chain length utilizing aliphatic dicarboxylic acid
304	4,553,507	Engine with additional shared flow control runner for two cylinders
305	4,543,816	Method and apparatus for monitoring the diameters of rod-shaped products of the tobacco processing industry
306	4,543,162	Multi-ply headbox having adjustable outlet slices
307	4,539,386	Process for forming thermally stable thermotropic liquid crystalline polyesters of predetermined chain length
308	4,538,979	Method of controlling a combustion flame
309	4,534,650	Device for the determination of the position of points on the surface of a body
310	4,533,245	Inspection lighting system
311	4,531,702	Injection mold for forming optical fiber connector
312	4,531,569	Process and apparatus for producing tubes of reactive metals
313	4,528,782	Sandblast nozzle
314	4,527,903	Apparatus for uniformizing the parameters of a flow and/or for mixing together at least two individual streams which discharge into a main flow

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315 4,522,940 Method of preparing a catalyst and catalyst prepared by the method
316 4,521,166 Inflatable air pump
317 4,520,723 Pressure roll for use in calenders or the like
318 4,512,282 Apparatus for coating plate-shaped bodies of glazed ceramic (tiles), glass or enamel
319 4,510,386 Thinning of specimens for examination under the electron microscope
320 4,505,053 Drying plant for a material web
321 4,498,786 Apparatus for mixing at least two individual streams having different thermodynamic functions of state
322 4,497,375 Force measuring apparatus mounted on tractor including Hall sensor detecting deformation of flex rod to control tractor power hoist
323 4,486,603 Preparation of trans cyclohexane 1,4-diamine
324 4,484,822 Method and apparatus for determining boiling points of liquids
325 4,477,583 Silica-modified catalyst and use for selective production of para-dialkyl substituted benzenes
326 4,477,328 Optically readable information disk and method of manufacturing same
327 4,467,114 Preparation of trans cyclohexane 1,4-diurea
328 4,465,886 Silica-modified catalyst and use for selective production of para-dialkyl substituted benzenes
329 4,464,675 Low frequency digital comb filter system
330 4,464,402 Process for manufacturing a high protein food material
331 4,459,466 Dual air passage heating apparatus with ceramic heater element
332 4,458,979 Light collecting arrangement in combination with a light scanning arrangement for inspecting a web of material
333 4,455,959 Apparatus for supporting the mast of a sailing board
334 4,449,278 Roller for supporting material sensitive to radiation and, method of making the same
335 4,432,962 Method for removing hydrogen sulfide from gas streams
336 4,432,214 Device for insertion and feed of products on the plates in a horizontal plate freezer
337 4,423,495 Method and apparatus for recording optically an information signal on a record medium along tracks
338 4,418,211 Preparation of trans-cyclohexane-1,4-disulphonyl urea
339 4,411,937 Process and composition for coating metals
340 4,402,822 Method of effecting highly exothermic reactions
341 4,399,981 Vessel for molten metal
342 4,392,546 Suspended operator station
343 4,377,085 Female dies and method of manufacture
344 4,374,526 Hearing faculty testing and apparatus therefor
345 4,365,746 Swirl injection valve
346 4,365,655 Flame retardant woven fabrics
347 4,356,010 Filter apparatus having filter elements and reverse-flow cleaning means
348 4,347,172 Process and composition for coating metals
349 4,335,316 Web break detector with adjustable scanning head
350 4,325,936 Method for removing hydrogen sulfide from gas streams

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	PAT. NO.	Title
351	4,323,077	Acoustic intensity monitor
352	4,315,510	Method of performing male sterilization
353	4,315,449	Cam operated cutoff machine
354	4,291,078	Breathable leather-like materials and process for making same
355	4,285,125	Barber-type razor
356	4,283,379	Method for removing hydrogen sulfide from gas streams
357	4,279,188	Acoustic coupling free electric drum
358	4,276,865	Diesel engine having a subchamber
359	4,251,724	Method and apparatus for determination of temperature, neutron absorption cross section and neutron moderating power
360	4,243,648	Method for removing hydrogen sulfide from gas streams
361	4,241,945	Motor vehicle bumper
362	4,241,856	Child-resistant fluid top
363	4,239,939	Stereophonic sound synthesizer
364	4,230,905	Stereophonic system with discrete bass channels
365	4,230,048	Railroad car
366	4,211,494	Device for guiding the printer needles in a mosaic needle printer
367	4,211,478	Circuit for indicating the condition of the battery in a photographic camera
368	4,210,115	Warm air intake system for an internal combustion engine

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369 4,206,012 Pick-up element for labels in a labeling machine
370 4,188,160 Feed residue saver for combines
371 4,188,027 Apparatus for laterally positioning sheets in printing machines or the like
372 4,183,120 Encircling devices
373 4,180,832 Video recording and reproducing apparatus having variable reproduction speeds
374 4,142,436 Method of playing stringed musical instrument
375 4,132,331 Collapsible packing tube
376 4,127,616 Process for selective production of para dialkyl substituted benzenes
377 4,120,551 Interlocking drawer assembly
378 4,115,646 Process for preparing 7-aminocephalosporanic acid derivatives
379 4,107,839 Manually guided cutting machine for sheet material
380 4,090,981 Catalyst for selective production of para dialkyl substituted benzenes
381 4,085,494 Method of and apparatus for positioning blades of a wood-chipping cutter drum
382 4,084,278 High speed transfer
383 4,081,739 Circuit for quick charging of batteries
384 4,079,999 Method and apparatus for mining
385 4,065,271 Process of separating hydrogen fluoride from gases
386 4,063,676 Friction welding methods and apparatus
387 4,058,176 Tool and method for drilling a hole with an increased cross-sectional area
388 4,054,844 Amplifying system
389 4,054,581 Preparation of cis-1-hydroxy-3-substituted-6,6-dimethyl-6,6a,7,8,10,10a-hexahydro-9H-dibenzo[b,d]pyran-9-ones and intermediates therefor
390 4,049,404 Ventilation system with thermal energy recovery
391 4,048,851 Axial and annular magneto-elastic dynamometers
392 4,041,379 Apparatus for testing metal blanks utilizing at least one inspecting head moved along the surface thereof
393 4,029,463 Method for baking food products
394 4,018,697 Fuel cycle management
395 4,014,472 Discharge nozzle structure
396 4,012,226 Process for steel production
397 4,008,648 Telescopic ram
398 3,999,395 Support arrangement for a construction
399 3,986,865 Process for producing steel
400 3,985,995 Method of making large structural one-piece parts of metal, particularly one-piece shafts

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Refine Search aclm/"substantially exclusively"

	PAT. NO.	Title
401	3,972,198	Method of protecting a pile imbedded in offshore areas having a shifting layer of mud
402	3,966,283	Refrigeration apparatus and method for making same
403	3,965,360	Method for discriminating high-temperature red heated material
404	3,958,619	Method for the separation of castings from casting moulds or similar material and a foundry machine for carrying out this method
405	3,949,894	Laminated container
406	3,948,052	Installation of an exhaust gas turbo-charger at an internal combustion engine
407	3,947,105	Production of colored designs
408	3,942,848	Shock absorbing pivot bearing for rotary watch parts

(12) RELATED PROCEEDINGS APPENDIX Page

There is no related proceeding.

CONCLUSION

with request for opinion under Board Rule 41.50(c):

In view of the foregoing information and analysis, the Appellant respectfully requests that the Board find patentable all of the claims presented on appeal herein, and instruct the Examiner to allow all those claims.

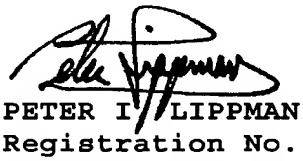
As noted earlier, Applicant requests the Board's permission to correct — after the appeal is concluded:

- the six minor errors in nomenclature that appear in claims 13 and 65; and also
- an error in claim 62 (its last paragraph should be conformed to claim 55, lines 9 through 13).

In event the Board disagrees with Appellant as to any of the claims, the Appellant earnestly asks that the Board provide, pursuant to Rule 41.50(c), "an explicit statement of how a claim on appeal may be amended to overcome [any] specific rejection".

The Applicant and the undersigned wish to thank the members of the Board for their patience in considering the many claims and many rejections in this case.

Respectfully submitted,



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